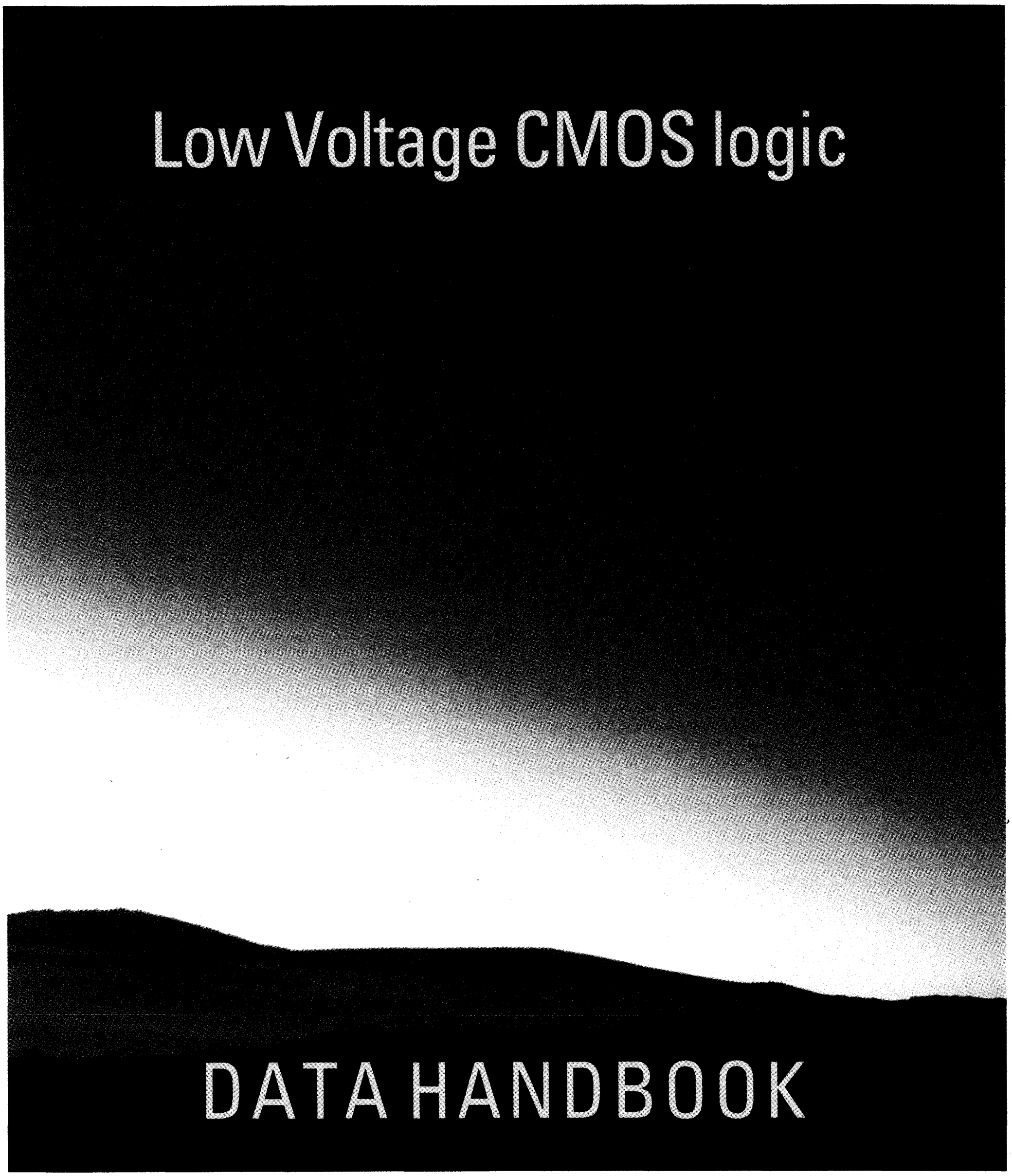
INTEGRATED CIRCUITS



Low Voltage CMOS logic

DATA HANDBOOK

BOOK IC24 1993

Philips Semiconductors

PHILIPS

LOW VOLTAGE CMOS LOGIC FAMILIES; HLL AND LV-HCMOS

Preface

Philips Semiconductors would like to thank you for your interest in our new low voltage CMOS logic families. The families HLL (High speed Low power Low voltage) and LV-HCMOS (Low Voltage High Speed CMOS) are optimized for applications working at 3.3 V, the standard supply voltage for may new digital systems. In addition they are guaranteed for operation at voltages as low as 1.2 V making them an ideal choice for many portable applications.

A detailed introduction to both new families can be found on page 3.

In addition to HLL and LV-HCMOS Philips Semiconductors offers the industry's most advanced line of logic products which, apart from a number of well established ranges of bipolar and CMOS families, include ABT (Advanced BiCMOS), MULTIBYTE™ and Futurebus+.

Philips Semiconductors shows a continuous innovation, bringing new product lines which are needed for novel designs.
Information regarding these and other families can be obtained from your nearest Philips Semiconductors' representative or authorized distributor.

Philips Semiconductors Logic ICs

Fast, low-power HLL & LV-HCMOS logic families

The heavy load imposed on electronic data processing (EDP) equipment by the ever-increasing complexity of modern software has led to the recent entry into the market of desktop computers and other EDP equipment using fast '386, '486, '586, 680x0 and RISC processors. This, in turn, has caused a demand for very fast low-power portable EDP equipment such as laptop computers, mobile radios, hand-held video games, telecom equipment and instrumentation.

To satisfy equipment manufacturers' component needs for this faster and/or lower power type of equipment, many new 3.3 V ICs such as the microprocessors mentioned above, static and dynamic memory, ASICs, disk controllers and flat-panel LCD controllers are now appearing on the market. This has added considerable momentum to the demand for fast, low-voltage 'glue logic' ICs to complete the chip-sets for fast, low-voltage EDP applications.

Philips has responded to this demand by developing the two new low-voltage CMOS logic families which are specified in this data handbook, to complement our existing range of logic ICs.
The new families are:
- HLL (High speed Low-power Low-voltage) logic

and
- LV-HCMOS (Low-Voltage High-speed CMOS) logic.

Both families have the wide supply voltage range (1.2 V to 3.6 V) and very low power consumption to make them an ideal choice for battery or mains-powered EDP applications where high speed and low power consumption are prime considerations.

REDUCING THE SUPPLY VOLTAGE FOR CMOS LOGIC WITHOUT LOSING SPEED

As shown in Fig.1, the power consumption of CMOS logic ICs diminishes approximately with the square of the supply voltage reduction. An obvious method of minimizing the power consumption of these circuits is therefore to reduce the conventional nominal supply voltage of 5 V to 3.3 V. Figure 1 shows that this reduction of supply voltage reduces the power consumption by about 65% and is accompanied by a speed reduction of only 20%. The immediate advantages gained simply by moving from 5 V to 3.3 V operation are therefore that the speed/power ratio for CMOS logic ICs is more than doubled, and it becomes possible to power them from a 1 or 2-cell battery in portable equipment.

The reduction of maximum speed resulting from the supply voltage reduction can be restored, and even increased, by using finer geometry and sub-micron CMOS technology which is tailored for low-power and low-voltage applications.

THE NEW HLL AND LV-HCMOS LOGIC FAMILIES FROM PHILIPS

We have used both supply voltage reduction and speed enhancement techniques for our new HLL and LV-HCMOS families of logic ICs.

Features common to both families are:
- Wide supply voltage range of 1.2 V to 3.6 V allows operation from a regulated mains-derived

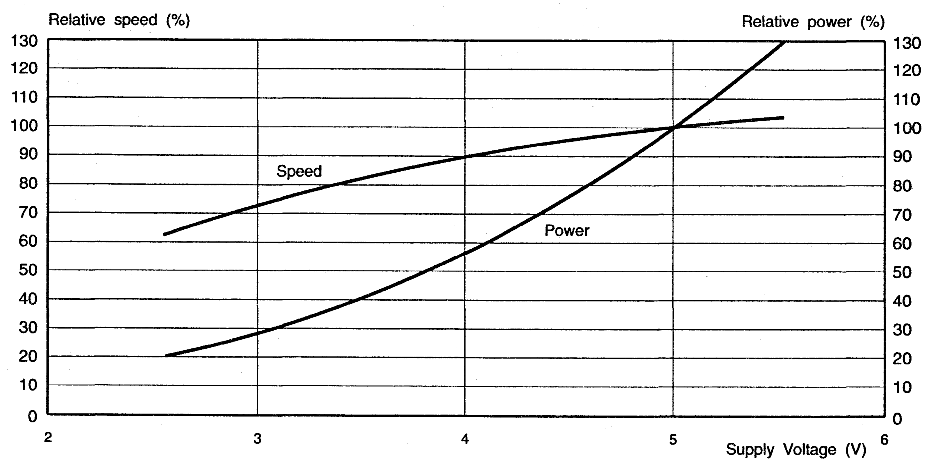


Fig.1 Normalized speed and power consumption of CMOS logic ICs. Reducing the supply voltage from 5 V to 3.3 V reduces speed to 80% and power consumption to 35%.

supply or an unregulated battery supply
- In accordance with the JEDEC LV standard (8.1) of 3.3 V ±0.3 V for ICs powered from a regulated supply
- Fabricated in CMOS for intrinsic low power consumption - only a few nanoamps of supply current flow in the static state
- Push-pull outputs that swing from rail to rail - the reduced voltage swing with a low-voltage supply reduces power consumption dramatically and also improves EMC and EMI; particularly important for portable RF equipment
- Minimal over-shoot and under-shoot noise
- Latch-up free operation
- Excellent ESD protection
- Low ground-bounce
- Improved system reliability due to lower power dissipation and minimized gate oxide thermal breakdown voltage
- Symmetrical waveforms
- Lowered power consumption allows:
  - ✓ smaller and lighter batteries
  - ✓ longer periods between battery charges
  - ✓ increased PCB packing density
  - ✓ reduced power supply costs

Features of the HLL family

HLL is an entirely newly designed logic family from Philips. It comprises extremely fast low-power logic ICs designed from scratch and fabricated in a sub-micron CMOS process with two-level metal and epitaxial substrates. HLL ICs with a 3.3 V ±0.3 V supply operate at twice the speed of FAST bipolar logic and, because they are CMOS ICs, they consume only a small fraction of the power. The family functions are mainly tailored for very high speed operation in the data-intensive bus interface area of mains-powered EDP equipment with a regulated 3.3 V supply. However, since they also function, at reduced speed (see Fig.2), with supply voltages down to as little as 1.2 V, HLL ICs can also be used in battery powered equipment.
Specific features of the HLL family are:
- Supply voltage 3.3 V ±0.3 V for maximum speed applications in equipment with regulated power supplies; 1.2 V to 3.6 V for battery powered equipment
- High dynamic output drive allows transition times to be much shorter than the propagation delay
- Sub-micron technology allows typical propagation delay of 2.5 ns with a 3.3 V supply - twice the speed of FAST with a 5 V supply
- Low-inductance, multiple centre power and ground pins for minimum noise and ground-bounce
- With a 3.3 V ±0.3 V supply, inputs and outputs interface directly with TTL levels
- Output edge-rate control circuitry for significantly less noise generation
- Reverse-biased diode (to ground only) at each input to limit line reflections
- The input voltage can exceed the supply voltage (up to 5.5 V), so HLL can be used for 5 V to 3 V and 3 V to 5 V level shifting in mixed 3 V/5 V systems
- SO and SSOP packages for surface mounting

Features of the LV-HCMOS family

This low-voltage CMOS logic family is based on Philips' well-known HCMOS (HC) range and uses the same well-proven fabrication process with only slight modifications. It operates from a typical supply voltage of 3.3 V but can be used within the supply voltage range 1.2 V to 3.6 V.
With a 3.3 V supply, the speed and performance is the same as HCMOS with a 5 V supply, so there are absolutely no disadvantages when replacing 5 V CMOS logic with LV-HCMOS.

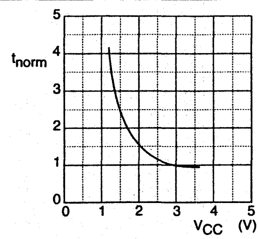


Fig.2 Normalized derating curve for typical propagation delay (t_P).

To obtain the speed and output drive of HCMOS at the lower supply voltage, the channel length for LV-HCMOS is reduced to 2 μm, the gate oxide is thinner and the threshold voltages are lowered. Functions are a sub-set of the HCMOS family functions.
Specific features of the LV-HCMOS family are:
- Process tuned for low-power applications with supply voltages between 1.2 V and 3.6 V
- Output drive at V_{CC} = 2 V is 4 mA (6 mA for driver outputs)
- Speed at 3 V is virtually the same as that of HCMOS at 5 V
- Faster than HCMOS at lower supply voltages
- Requires minimal qualification by the user because it is produced in our established HCMOS wafer fab. with a process that varies little from the standard HCMOS process
- Pin- and function-compatible with HCMOS ICs
- Identical high quality standards as for all Philips' HCMOS ICs.
- SO and SSOP packages for surface mounting

SUPPLY VOLTAGE CONSIDERATIONS

There are three main reasons for reducing the supply voltage of logic ICs:
- To allow them to be used in portable battery powered equipment
- To reduce power consumption

(dissipation) so that the size and weight of equipment can be reduced and portable equipment can function for longer periods without re-charging the battery
- To meet demands for faster, high-performance operation, ICs must be fabricated with finer process geometry which requires a lower supply voltage.

Other benefits of a low supply voltage include lower noise levels, reduced EMI, and improved reliability due to reduced stresses on the ICs.

There is not yet a well-defined industry standard for low-voltage operation, but a level of 3.3 V ±0.3 V seems to be common for equipment with a regulated supply and is also proposed by JEDEC. For battery operation, the requirements are more stringent because the supply voltage variation is greater. For example, at the end of their operating life, a pair of Alkaline or Carbon Zinc batteries can only supply about 1.8 V, and a single NiCd cell provides only 1.2 V just before it needs re-charging. The wide supply voltage range and output drive levels of HLL and LV-HCMOS ICs allows them to be powered from any of these sources.

POSITIONING OF HLL AND LV-HCMOS WITH RESPECT TO OTHER LOGIC FAMILIES

Figures 3, 4 and 5 are included here for clarification purposes only.

Figure 3 shows speed as a function of supply voltage for Philips CMOS logic IC families. Figure 4 shows the speed of most advanced logic families compared to the speed of FAST logic ICs.

Figure 5 shows power consumption as a function of speed for an octal transceiver from various logic families. Each output of the IC is loaded with 50 pF and the eight transceivers in the device are each driven by one bit of an 8-bit binary code that counts from 00000000 to 11111111. The transceiver driven by the least-significant bit is therefore running at the highest frequency, and the transceiver driven with the most-significant bit is running at a frequency 2^7 times lower.

The HLL family

Figure 3 shows that the extreme speed of HLL makes it a clear extension to Philips' range, complementing our other logic families. Users needing low power consumption or with data-intensive applications can derive full benefit from HLL.
Figure 4 indicates that the speed of HLL is exceptional when compared to other logic families. As is common practice, the speeds in Fig.4 are referenced to FAST logic. By attempting to emulate, or even improve on FAST logic speed, many new logic families appearing on the market put signal integrity at stake. This is why Philips believes that the proven low-impedance multiple centre power supply pinning used for HLL will become an industry standard for very fast logic. The background for this is the effect of groundbounce. Groundbounce not only affects signal integrity, it also affects the propagation delays when all outputs are switching. It is simply impossible to make CMOS devices with corner pin which combine the extreme speeds as provided by HLL during simultaneous switching. In addition centre-pin devices provide low skew and improved EMC.

As expected for CMOS products with their intrinsic low static power consumption, Fig.5 shows that, in the idle state and at low frequencies, HLL ICs consume negligible power. In the idle state, power consumption is only 0.25 mW, and at 1 MHz it is a mere 0.9 mW. This makes HLL very attractive for applications where short propagation delays are essential and low dissipation is required. With a 3 V supply at 100 MHz, power consumption for

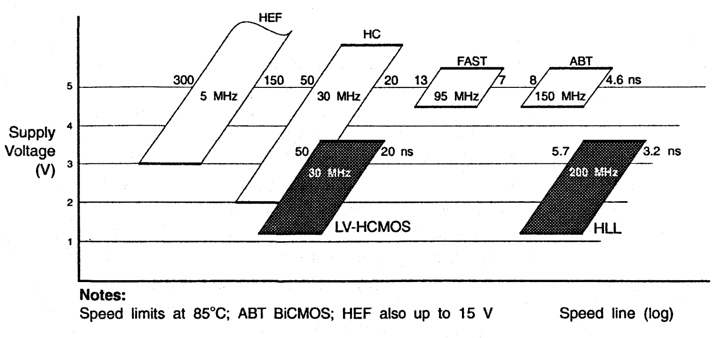


Fig.3 Guaranteed speed as a function of supply voltage for Philips logic ICs. The speed range per logic family is due to the different functions within the families.

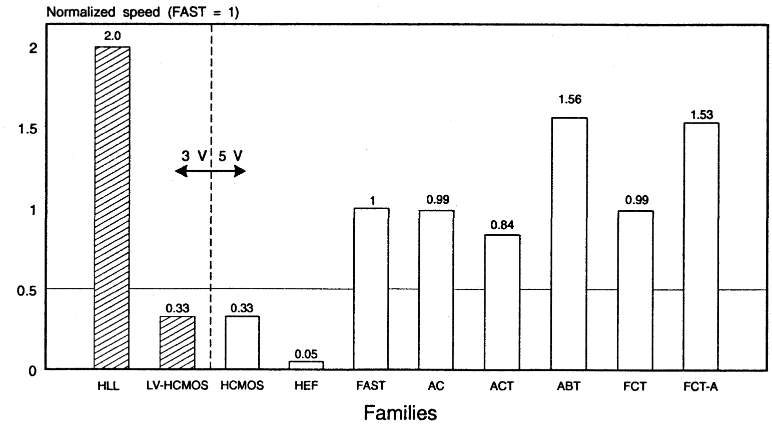


Fig.4 Speed of various logic families compared with the speed of FAST logic.

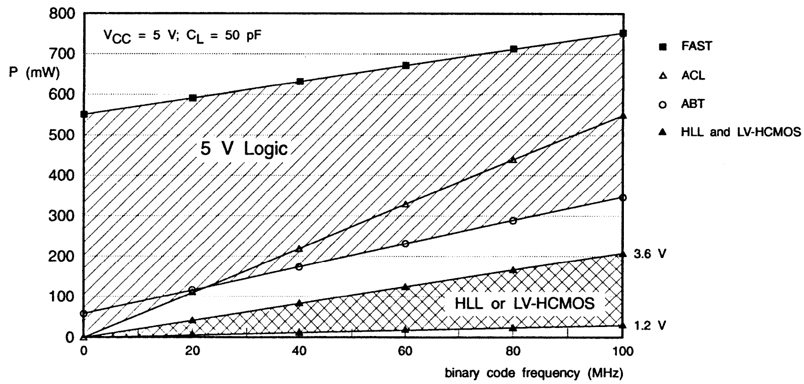


Fig.5 Power consumption of an octal transceiver ('245) as a function of frequency for various logic families.

HLL is between 60% and 80% less than for other advanced 5 V logic families.

The LV-HCMOS family

From Fig.3 and Fig.4, it can be seen that, with a 3.3 V supply, LV-HCMOS offers the same familiar speeds of HC HCMOS ICs with a 5 V supply. This allows 3.3 V ±0.3 V systems to be designed with the same speed and performance as 5 V ±10% systems using HCMOS HC ICs. The tremendous advantage of using LV-HCMOS, considerably lower power consumption, is clearly shown in Fig.5. With a 3 V supply at 30 MHz, an LV-HCMOS octal transceiver consumes 70% less power than a similar advanced CMOS device. At lower supply voltages, the power savings are even greater.

INTERFACING IN MIXED 3 V / 5 V SYSTEMS

CMOS ICs like HLL and LV-CMOS have considerable benefits with respect to noise margins because, unlike with bipolar ICs, there is hardly any voltage drop across the output devices. This means that the outputs swing virtually between the power supply rails, thereby allowing direct interfacing with TTL switching levels.

When interfacing HLL or LV-HCMOS outputs with standard TTL-compatible level logic inputs, the outputs of HLL and LV-HCMOS are adequate to directly drive the 5 V logic. When driving CMOS level devices (such as AC or HC) the output voltage of

HLL and LV-HCMOS is insufficient to ensure reliable operation. This problem can be easily resolved by using TTL-compatible HCMOS ICs (ACT or HCT) at the interface.

Since HLL inputs can withstand higher levels than the supply voltage, they can be directly connected to 5 V CMOS logic outputs.

LV-HCMOS devices have a protection diode between the input and V_{CC}. This implies that the maximum input voltage is limited to V_{CC} + 0.5 V.
When LV-HCMOS is driven by 5 V outputs having a TTL (totem-pole) compatible output voltage swing of about 3 V, direct drive is possible. However, when full 5 V output voltage swing devices are used, such as CMOS ASICs or CMOS logic, problems may occur. In such case a simple resistor-diode network or the use of open drain devices can provide a solution (see Fig. 6). Alternatively, HLL ICs can be used as 5 V/3 V level converters for connecting 5 V CMOS logic outputs to LV-HCMOS inputs.

PHILIPS FOR ADVANCED LOGIC ICs

Our two new low-voltage CMOS logic families LV-HCMOS and HLL are only a small part of Philips' total portfolio which includes a wide range of advanced bipolar, CMOS and QUBIC (BiCMOS) logic ICs.

Continuity of supply from Philips is assured, thanks to our own global manufacturing/distribution organization, and to our alternate sourcing agreements for many products.

Philips' wafer fabrication plants and IC assembly factories are located close to market centres throughout the world. The continual extension of these facilities clearly demonstrates that Philips operates on a global scale, and is committed to growth in virtually all countries. Ship-to-stock arrangements and Self-Qual programmes (which provide information about qualification activities for new/changed products/processes) are just two of the special customer services we can offer. Naturally, we also offer design-in support and technical assistance. Since Philips' technical expertise embraces a broad spectrum of application areas, we can offer you invaluable help with your product designs. Maintaining a close and open relationship with our customers helps us to optimize our design-ins.

QUALITY AND RELIABILITY OF PHILIPS' PRODUCTS

All Philips' products are of a high quality, constantly enhanced by a system of continuous quality improvement. We start to achieve our high level of quality during development of new devices by including staff from our Quality Department in the development teams. Testing includes life testing (including HAST) and thermal shock. We use sound methods of managing product reliability improvement to ensure that our products continue to perform to their specifications. Up-to-date quality reports are available to customers.

Over the years, Philips has proved itself to be a reliable supplier and our commitment to quality has been underlined by the many awards received in honour of outstanding achievements in this field. These awards include:

- The ISO 9001 qualification
- Qualified supplier to Hewlett Packard, Bosch, Canon, Chrysler, Delco, IBM cat. I & II and others
- The Ford Q1 award with consistently high scores
- The Bull Quality Award 1991
- Siemens' 'Best IC supplier' of 1989
- Unisys Oscar 1990.

More specific information about Philips' Quality Programme can be found in the chapter on Quality on page 17.

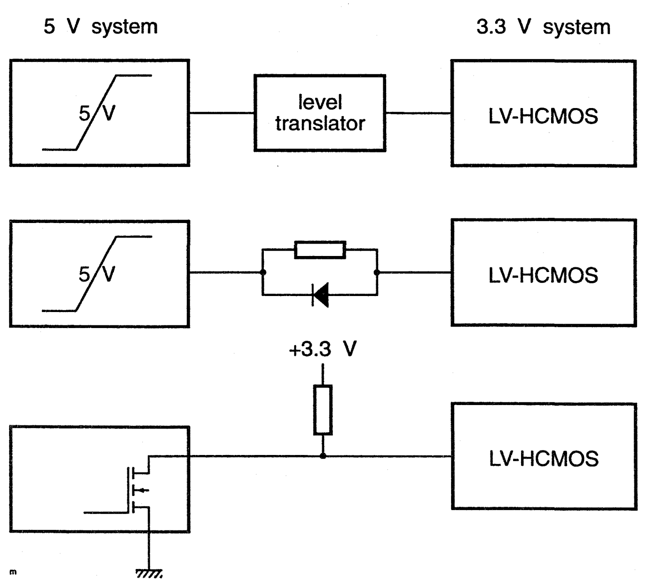


Fig.6 Interfacing 5 V systems to LV-HCMOS.

74HLL family

LV-HCMOS family

Ordering Information

TYPE NUMBER DESIGNATIONS

HLL RANGE

74 HL 33 XXX X

- X — Package code
  D = plastic surface mount device (SO)
  DB = small plastic suface mount device (SSOP)
- XXX — three character device code
  (functionally compatible to HC/HCT code)
- 33 — pinout designator; centre V_{cc}/GND pins
- HL — HL = HLL family
- 74 — 74 = commercial operating temperature range; -40° to +85°

LV RANGE

74 LV XXX X

- X — Package code
  N = plastic Dual-In-Line (DIL)
  D = plastic surface mount device (SO)
  DB = small plastic surface mount device (SSOP)
- XXX — three character device code
  (functionally compatible to HC/HCT code)
- LV — LV = LV-HCMOS family
- 74 — 74 = commercial operating temperature range; -40° to +85°

FAMILY DESCRIPTION

The HLL family comprises extremely fast low-power logic ICs fabricated in a sub-micron CMOS process with two-level metal and epitaxial substrates. HLL ICs with 3.3 V ±0.3 V supply operates at twice the speed of FAST bipolar logic and consumes only a fraction of the power. The HLL functions with supply voltages down to 1.2 V. The reduction from the conventional 5.0 V to 3.3 V reduces the output swing dramatically and this with the low-inductance multiple centre power and ground pins significantly reduces noise and ground bounce that would otherwise occur for signals with this very high speed.

RECOMMENDED OPERATING CONDITIONS FOR THE HLL FAMILY

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage (for max. speed performance)	3.0	3.6	V	
V_{CC}	DC supply voltage (for low-voltage applications)	1.2	3.6	V	
V_I	DC input voltage range	0	5.5	V	
$V_{I/O}$	DC input voltage range for I/Os	0	V_{CC}	V	
V_O	DC output voltage range	0	V_{CC}	V	
T_{amb}	operating ambient temperature range in free air	−40	+85	°C	see DC and AC characteristics per device
t_r, t_f	input rise and fall times	– –	20 50	ns ns	V_{CC} = 3.6 V V_{CC} = 1.2 V

LIMITING VALUES FOR THE HLL FAMILY

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+4.6	V	
I_{IK}	DC input diode current	–	−50	mA	$V_I < 0$
V_I	DC input voltage	−0.5	+5.5	V	note 2
$V_{I/O}$	DC input voltage range for I/Os	−0.5	V_{CC} + 0.5	V	
I_{OK}	DC output diode current	–	±75	mA	$V_O > V_{CC}$ or $V_O < 0$
V_O	DC output voltage	−0.5	V_{CC} + 0.5	V	note 2
I_O	DC output source or sink current	–	±70	mA	V_O = 0 to V_{CC}
I_{GND}, I_{CC}	DC V_{CC} or GND current	–	100	mA	
T_{stg}	storage temperature range	−60	+150	°C	
P_{tot}	power dissipation per package - plastic mini-pack (SO)	–	500	mW	above + 70 °C derate linearly with 8 mW/K

Notes to the limiting values

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operating of the device at these or any other conditions beyond those under 'recommended operating conditions' is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR THE HLL FAMILY

Over recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)					UNIT	TEST CONDITIONS		
		+25			−40 to +85			V_{CC} (V)	V_I	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.				
V_{IH}	HIGH level input voltage	–	–	–	2.0	–	V	3.6		
V_{IL}	LOW level input voltage	–	–	–	–	0.8	V	3.0		
V_H	hysteresis (all inputs)	–	0.25	–	–	–	V	3.0 to 3.6		
V_{OH}	HIGH level output voltage	V_{CC} – 0.2 V_{CC} – 0.4	V_{CC} –	– –	V_{CC} – 0.2 V_{CC} – 0.4	– –	V	3.0	V_{IH} or V_{IL}	I_O = −100 μA I_O = −24 mA
V_{OL}	LOW level output voltage	– –	– –	0.2 0.4	– –	0.2 0.4	V	3.0	V_{IH} or V_{IL}	I_O = 100 μA I_O = 24 mA
I_I	input leakage current	–	–	–	–	±5	μA	3.6	V_{CC} or GND	
I_{OZ}	3-state output OFF-state current	–	–	–	–	10	μA	3.6	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current	–	–	8.0	–	80	μA	3.6	V_{CC} or GND	I_O = 0

The LV-HCMOS family

Please note that there is only one LV-HCMOS family and all the ICs are suitable for operation over the temperature range −40 °C to +125 °C. However, as a reference for system designers, and to facilitate comparison with other logic families, the performance of LV-HCMOS ICs is specified at 25 °C and over the temperature ranges −40 °C to +85 °C and −40 °C to +125 °C.

RECOMMENDED OPERATING CONDITIONS FOR THE LV-HCMOS FAMILY

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	1.2	3.3	3.6	V	
V_I	input voltage	0	–	V_{CC}	V	
V_O	output voltage	0	–	V_{CC}	V	
T_{amb}	operating ambient temperature range in free air	−40 −40	– –	+85 +125	°C	see DC and AC characteristics per device
t_r, t_f	input rise and fall times except for Schmitt-trigger inputs	– – – –	– – – –	1000 700 500 400	ns	V_{CC} = 1.2 V V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 3.6 V

ABSOLUTE MAXIMUM RATINGS FOR THE LV-HCMOS FAMILY

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+5.0	V	
$\pm I_{IK}$	DC input diode current	–	20	mA	$V_I < -0.5$ or $V_I > V_{CC} +0.5$ V
$\pm I_{OK}$	DC output diode current	–	50	mA	$V_O < -0.5$ or $V_O > V_{CC} +0.5$ V
$\pm I_O$	DC output source or sink current - standard outputs - bus driver outputs	 – –	 25 35	mA	$-0.5\text{ V} < V_O < V_{CC} + 0.5$ V
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with - standard outputs - bus driver outputs	 – –	 50 70	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package - plastic DIL	–	750	mW	for temperature range: −40 to +125 °C above + 70 °C derate linearly with 12 mW/K
	- plastic mini–pack (SO)	–	500	mW	above + 70 °C derate linearly with 8 mW/K

Notes to the limiting values

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operating of the device at these or any other conditions beyond those under 'recommended operating conditions' is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS FOR THE LV-HCMOS FAMILY

Over recommended operating conditions
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C) +25 MIN.	+25 TYP.	+25 MAX.	−40 to +85 MIN.	−40 to +85 MAX.	−40 to +125 MIN.	−40 to +125 MAX.	UNIT	TEST CONDITIONS V_{CC} (V)	V_I	OTHER
V_{IH}	HIGH level input voltage	0.9 1.4 2.1	– – –	– – –	0.9 1.4 2.1	– – –	0.9 1.4 2.1	– – –	V	1.2 2.0 3.0		
V_{IL}	LOW level input voltage	– – –	– – –	0.3 0.6 0.9	– – –	0.3 0.6 0.9	– – –	0.3 0.6 0.9	V	1.2 2.0 3.0		
V_{OH}	HIGH level output voltage; all outputs	1.1 1.9 2.9	1.2 2.0 3.0	– – –	1.0 1.9 2.9	– – –	1.0 1.9 2.9	– – –	V	1.2 2.0 3.0	V_{IH} or V_{IL}	$-I_O$ = 50 μA
V_{OH}	HIGH level output voltage; standard outputs	2.48	2.82	–	2.34	–	2.20	–	V	3.0	V_{IH} or V_{IL}	$-I_O$ = 6 mA
V_{OH}	HIGH level output voltage; bus driver outputs	2.48	2.82	–	2.34	–	2.20	–	V	3.0	V_{IH} or V_{IL}	$-I_O$ = 8 mA
V_{OL}	LOW level output voltage; all outputs	– – –	0 0 0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V	1.2 2.0 3.0	V_{IH} or V_{IL}	I_O = 50 μA
V_{OL}	LOW level output voltage; standard outputs	–	0.25	0.33	–	0.4	–	0.5	V	3.0	V_{IH} or V_{IL}	I_O = 6 mA
V_{OL}	LOW level output voltage; bus driver outputs	–	0.20	0.33	–	0.4	–	0.5	V	3.0	V_{IH} or V_{IL}	I_O = 8 mA
I_I	input leakage current	–	–	0.1	–	1.0	–	1.0	μA	3.6	V_{CC} or GND	
I_{OZ}	3-state output OFF-state current	–	–	0.5	–	5.0	–	10.0	μA	3.6	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current; SSI flip-flops MSI	 – – –	 – – –	 2.0 4.0 8.0	 – – –	 20.0 40.0 80.0	 – – –	 40.0 80.0 160.0	μA	3.6	V_{CC} or GND	I_O = 0

AC OUTPUT CHARACTERISTICS FOR THE LV-HCMOS FAMILY

SYMBOL	PARAMETER	T_{amb} (°C) +25 MIN.	+25 TYP.	+25 MAX.	−40 to +85 MIN.	−40 to +85 MAX.	−40 to +125 MIN.	−40 to +125 MAX.	UNIT	TEST CONDITIONS V_{CC} (V)	WAVEFORMS
t_{THL}/t_{TLH}	transition time; standard outputs	– – –	35 10 7	– 20 15	– – –	– 25 19	– – –	– 30 23	ns	1.2 2.0 3.0	
t_{THL}/t_{TLH}	transition time; bus driver outputs	– – –	25 8 5	– 16 10	– – –	– 20 13	– – –	– 24 15	ns	1.2 2.0 3.0	

DEFINITIONS OF SYMBOLS AND TERMS USED IN DATA SHEETS

Currents

Positive current is defined as conventional current flow into a device.
Negative current is defined as conventional current flow out of a device.

I_{CC}	Quiescent power supply current; the current flowing into the V_{CC} supply terminal.
ΔI_{CC}	Additional quiescent supply current per input pin at a specified input voltage and V_{CC}.
I_{GND}	Quiescent power supply current; the current flowing into the GND terminal.
I_I	Input leakage current; the current flowing into a device at a specified input voltage and V_{CC}.
I_{IK}	Input diode current; the current flowing into a device at a specified input voltage.
I_O	Output source or sink current; the current flowing into a device at a specified output voltage.
I_{OK}	Output diode current; the current flowing into a device at a specified output voltage.
I_{OZ}	OFF-state output current: the leakage current flowing into the output of a 3-state device in the OFF-state, when the output is connected to V_{CC} or GND.
I_S	Analog switch leakage current; the current flowing into an analog switch at a specified voltage across the switch and V_{CC}.

Voltages

All voltages are referenced to GND (ground), which is typically 0 V.

GND	Supply voltage; for a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages; typically ground.
V_{CC}	Supply voltage; the most positive potential on the device.
V_{EE}	Supply voltage; the one of two (GND and V_{EE}) negative power supplies.
V_H	Hysteresis voltage; difference between the trigger levels, when applying a positive and negative-going input signal.
V_I	DC input voltage
$V_{I/O}$	DC input voltage for I/Os
V_{IH}	HIGH level input voltage; the range of input voltages that represents a logic HIGH level in the system.
V_{IL}	LOW level input voltage; the range of input voltages that represents a logic LOW level in the system.
V_{OH}	HIGH level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a HIGH level at the output.
V_{OL}	LOW level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a LOW level at the output.
V_{T+}	Trigger threshold voltage; positive-going signal.
V_{T-}	Trigger threshold voltage; negative going signal.

Analog terms

R_{ON}	ON-resistance; the effective ON-state resistance of an analog switch, at a specified voltage across the switch and output load.
ΔR_{ON}	ΔON-resistance; the difference in ON-resistance between any two switches of an analog device at a specified voltage across the switch and output load.

Capacitances

C_I	Input capacitance; the capacitance measured at a terminal connected to an input of a device.
$C_{I/O}$	Input/Output capacitance; the capacitance measured at a terminal connected to an I/O-pin (e.g. a transceiver).
C_L	Output load capacitance; the capacitance connected to an output terminal including jig and probe capacitance.
C_{PD}	Power dissipation capacitance; the capacitance used to determine the dynamic power dissipation per logic function, when no extra load is provided to the device.
C_S	Switch capacitance; the capacitance of a terminal to a switch of an analog device.

AC switching parameters

f_i	Input frequency; for combinatorial logic devices the maximum number of inputs and outputs switching in accordance with the device function table. For sequential logic devices the clock frequency using alternate HIGH and LOW for data input or using the toggle mode, whichever is applicable.
f_o	Output frequency; each output.
f_{max}	Maximum clock frequency; clock input waveforms should have a 50% duty factor and be such as to cause the outputs to be switching from 10%V_{CC} to 90%V_{CC} in accordance with the device function table.
t_h	Hold time; the interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their continued recognition. A negative hold time indicates that the correct logic level may be released prior to the timing pulse and still be recognized.
t_r, t_f	Clock input rise and fall times; 10% and 90% values.
t_{PHL}	Propagation delay; the time between the specified reference points, normally the 50% points for logic devices on the input and output waveforms, with the output changing from the defined HIGH level to the defined LOW level.
t_{PLH}	Propagation delay; the time between the specified reference points, normally the 50% points for logic devices on the input and output waveforms, with the output changing from the defined LOW level to the defined HIGH level.
t_{PHZ}	3-state output disable time; the time between the specified reference points, normally the 50% points for the logic devices on the output enable input voltage waveform and a point representing 10% of the output swing on the output voltage waveform of a 3-state device, with the output changing from a HIGH level (V_{OH}) to a high impedance OFF-state (Z).
t_{PLZ}	3-state output disable time; the time between the specified reference points, normally the 50% points for the logic devices on the output enable input voltage waveform and a point representing 10% of the output swing on the output voltage waveform of a 3-state device, with the output changing from a LOW level (V_{OL}) to a high impedance OFF-state (Z).
t_{PZH}	3-state output enable time; the time between the specified reference points, normally the 50% points for the logic devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state (Z) to a HIGH level (V_{OH}).
t_{PZL}	3-state output enable time; the time between the specified reference points, normally the 50% points for the logic devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state (Z) to a LOW level (V_{OL}).
t_{rem}	Removal time; the time between the end of an overriding asynchronous input, typically a clear or reset input, and the earliest permissible beginning of a synchronous control input, typically a clock input, normally measured at the 50% points for logic devices on both input voltage waveforms.
t_{su}	Set-up time; the interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.
t_{THL}	Output transition time; the time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from HIGH-to-LOW.
t_{TLH}	Output transition time; the time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from LOW-to-HIGH.
t_W	Pulse width; the time between the 50% amplitude points on the leading and trailing edges of a pulse for the logic family devices

QUALITY AT PHILIPS SEMICONDUCTORS

Total Quality Management

Philips Semiconductors are a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is:

QUALITY ASSURANCE

based on ISO 9000 standards, customer standards such as Ford Q1 and IBM MDQ, and the CECC system of conformity. Our factories are certified to ISO 9000 and CECC by external inspectorates

PARTNERSHIPS WITH CUSTOMERS

PPM co-operations, design-in agreements, and ship-to-stock, just-in-time and self-qualification programmes

PARTNERSHIPS WITH SUPPLIERS

ship-to-stock, statistical process control and ISO 9000 audits

QUALITY IMPROVEMENT PROGRAMME

continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

Advanced quality planning

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

Product conformance

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- incoming material management through partnerships with suppliers
- in-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control
- acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications
- periodic inspections to monitor and measure the conformance of products.

Product reliability

With the increasing complexity of OEM (original equipment manufacturer) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies have resulted in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

Customer responses

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Electrostatic charges

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

Work station

Fig.1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ; per cm^2. The floor should also be covered with antistatic material.

The following precautions should be observed:

- persons at a work bench should be earthed via a wrist strap and a resistor
- all mains-powered electrical equipment should be connected via an earth leakage switch
- equipment cases should be earthed
- relative humidity should be maintained between 50 and 65%
- an ionizer should be used to neutralize objects with immobile static charges.

Receipt and storage

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

Assembly

MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken. During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.

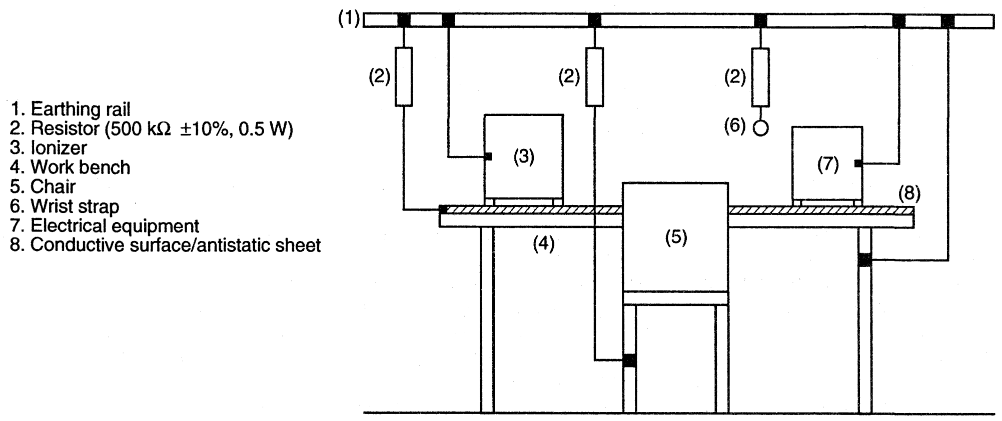
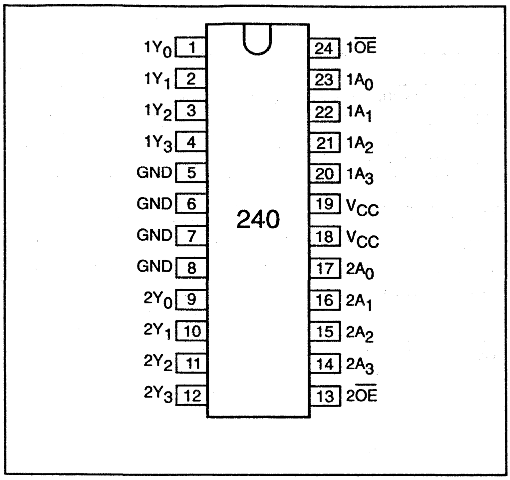


Fig.1 Protected work station.

Definition of data sheet status

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operating of the device at these or any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	



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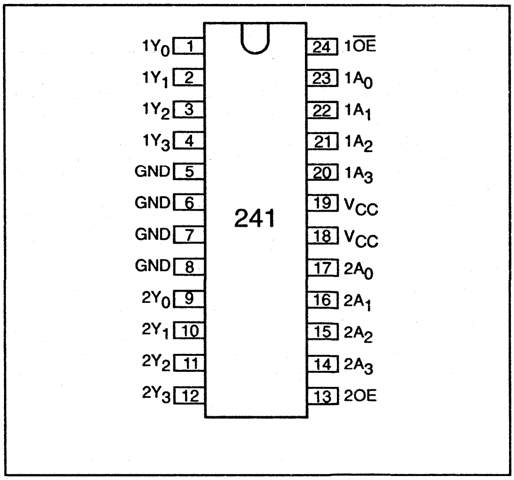

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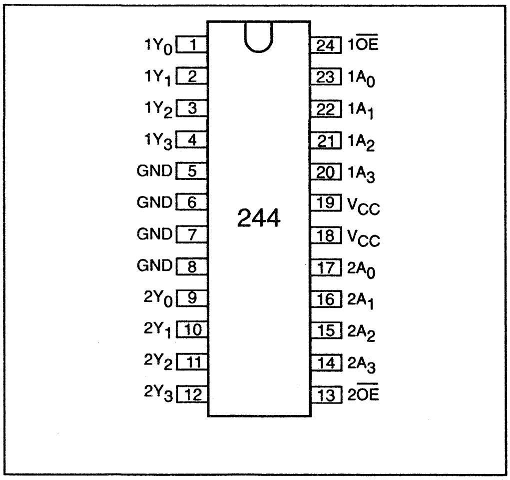

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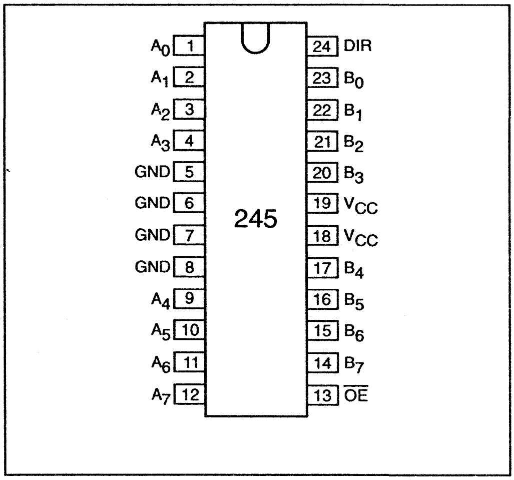

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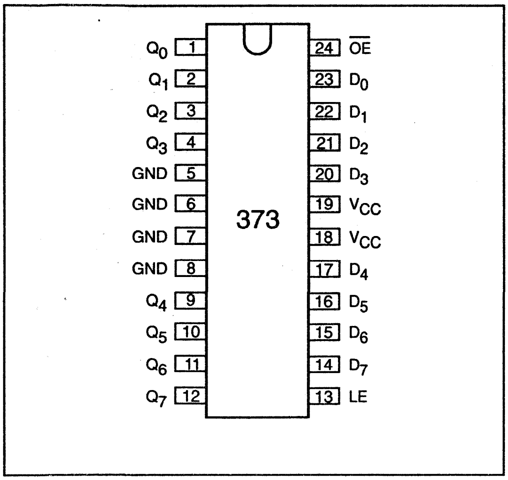

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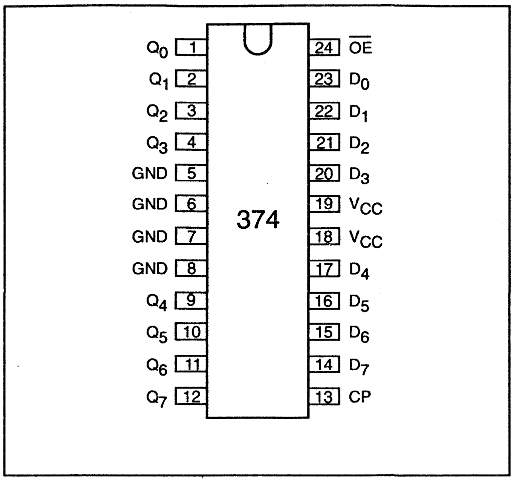

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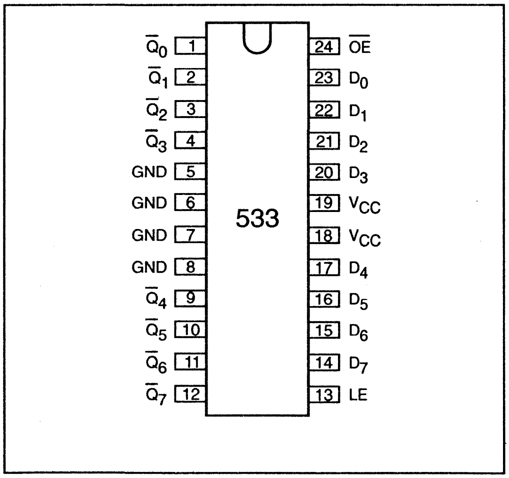

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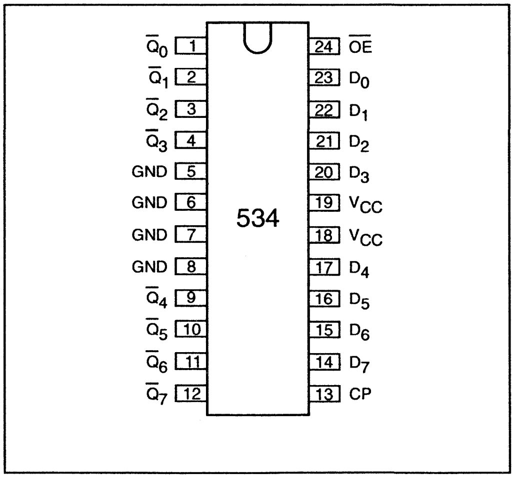

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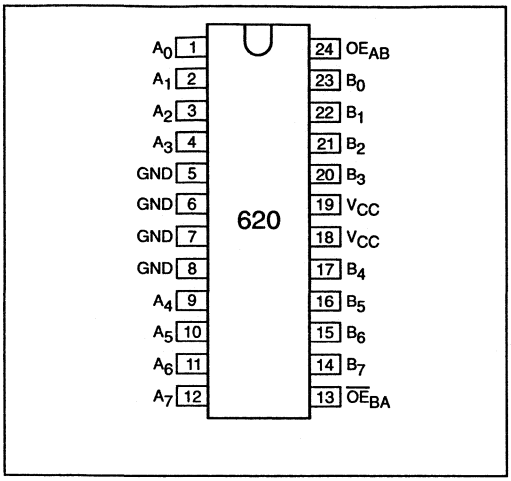

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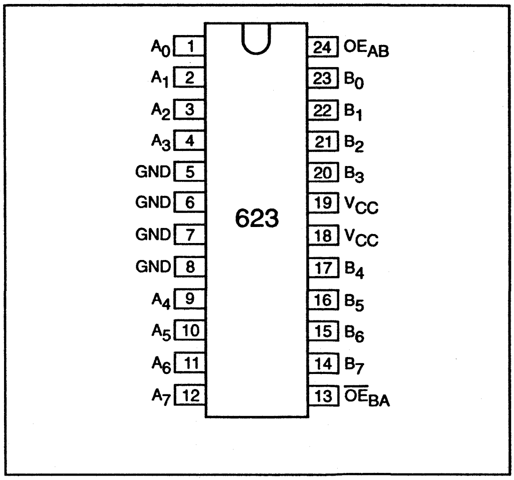

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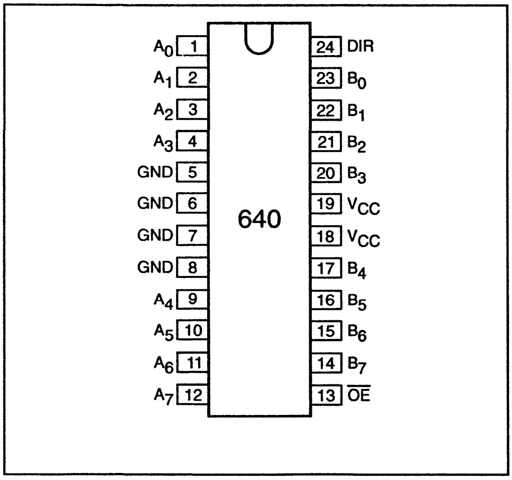

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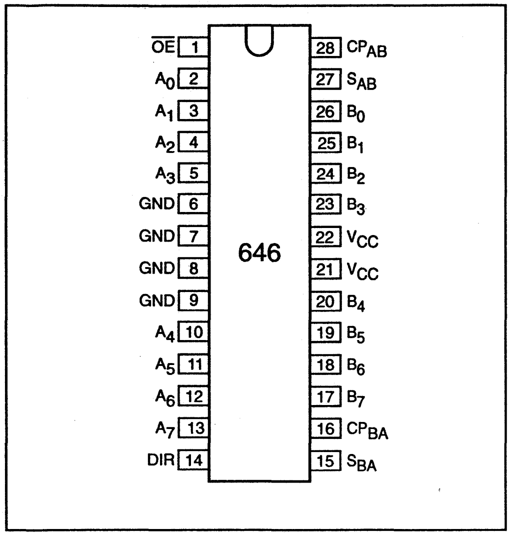

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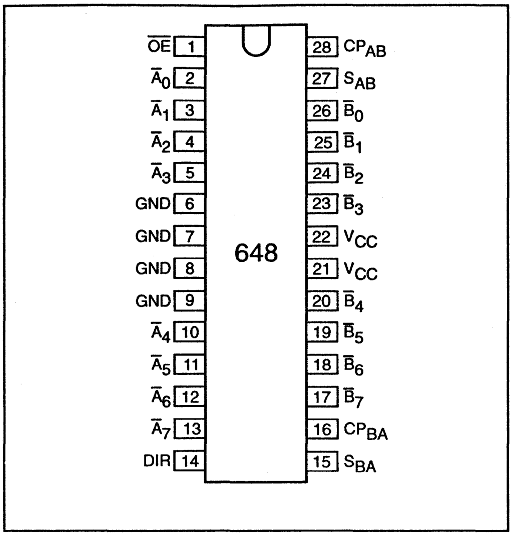

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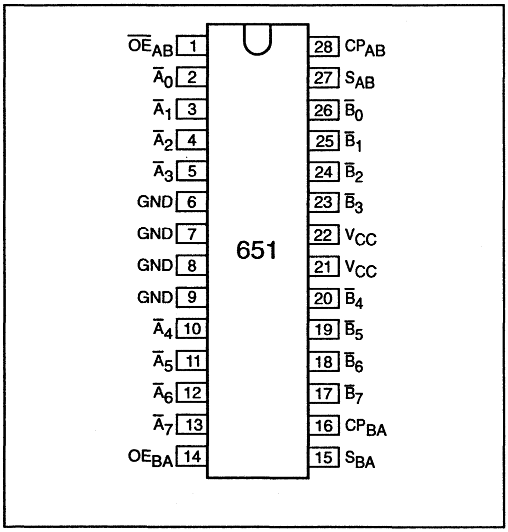

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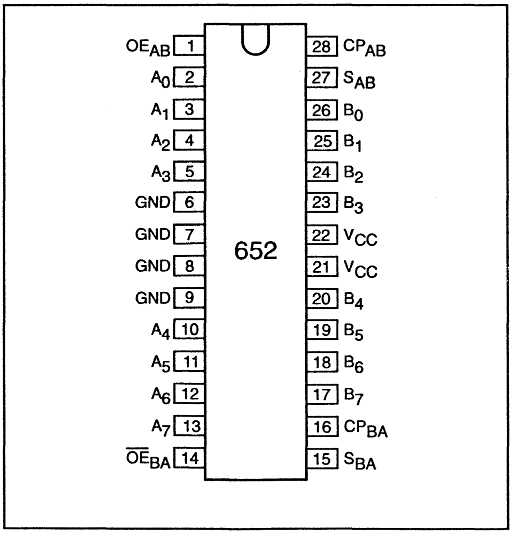

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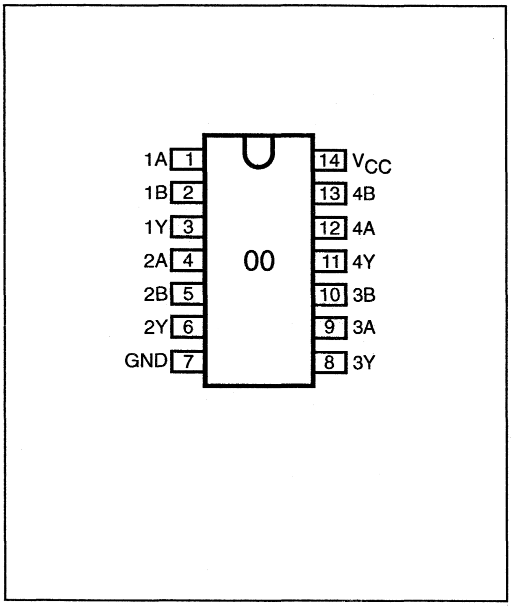

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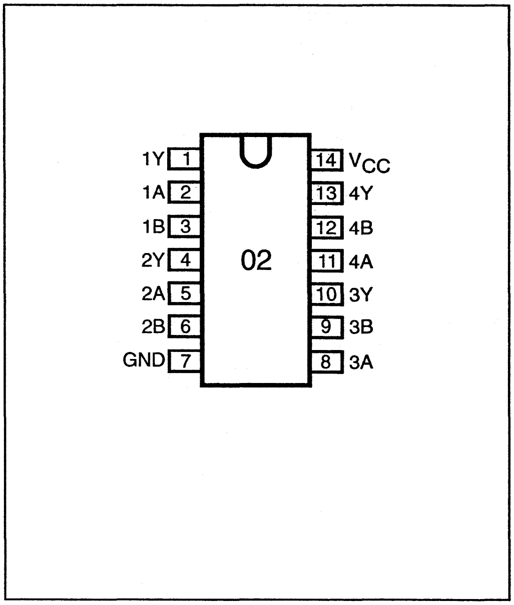

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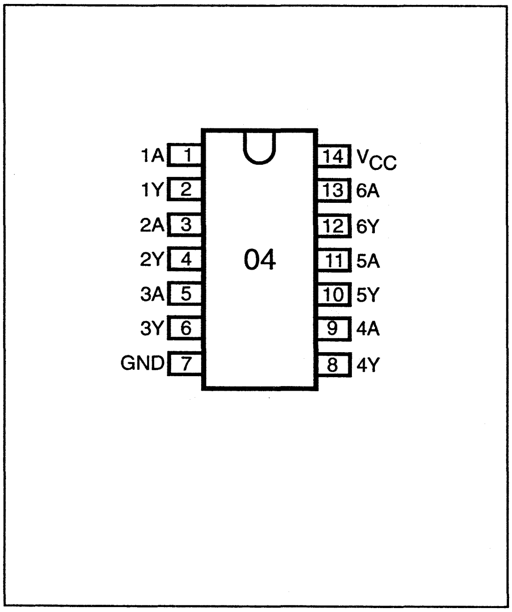

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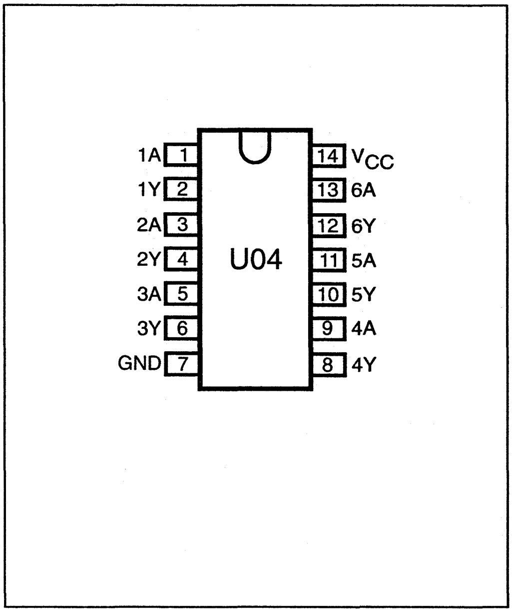

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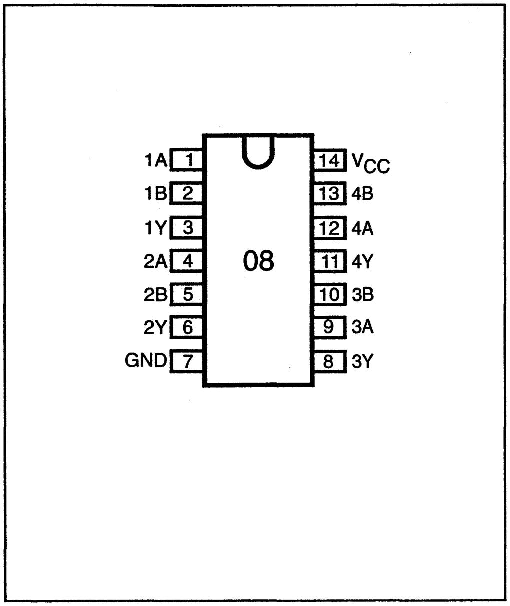

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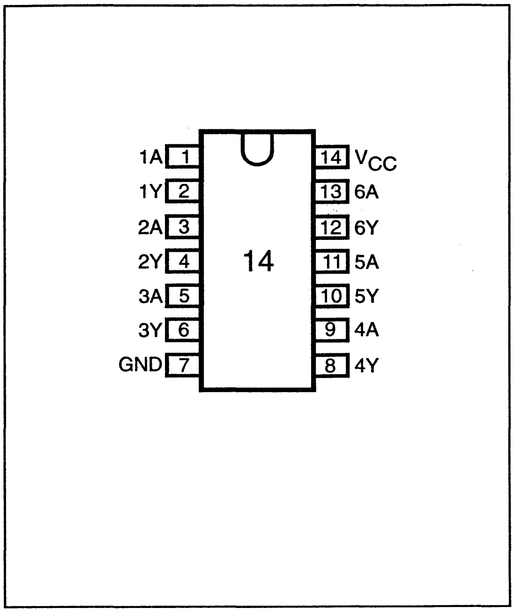

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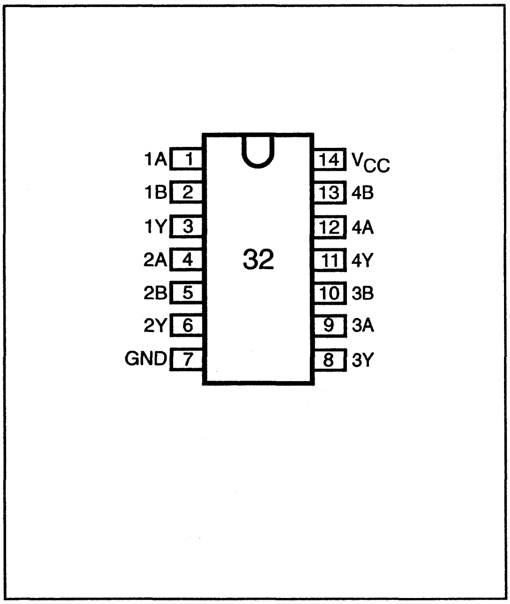

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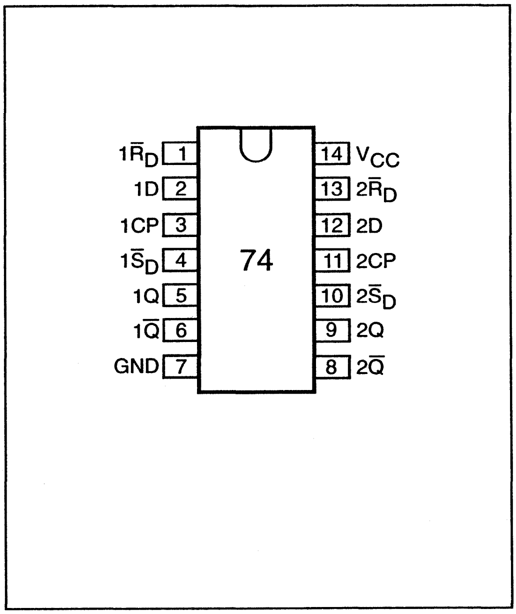

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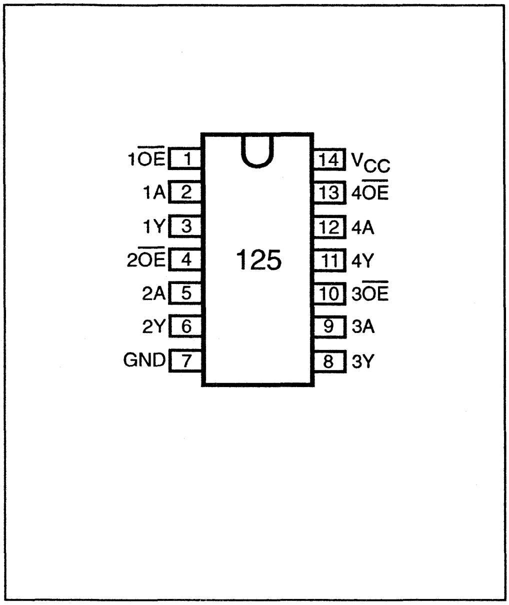

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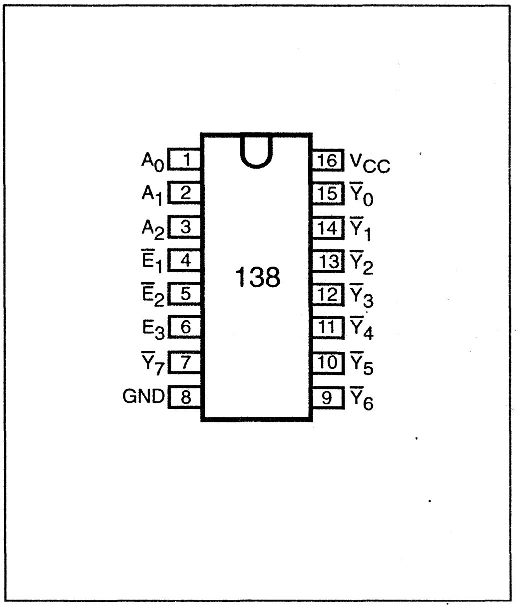

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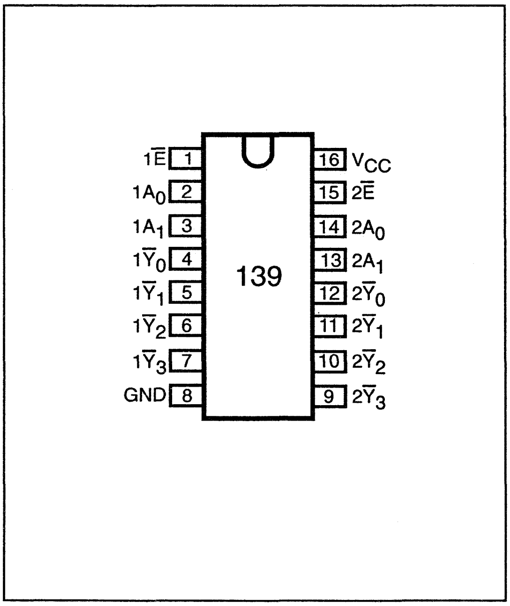

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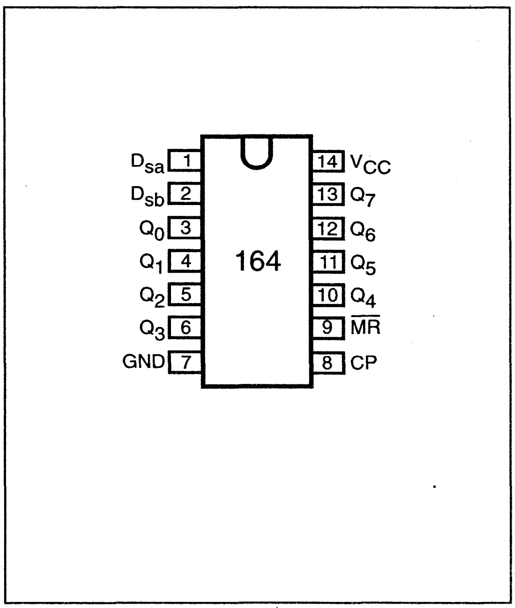

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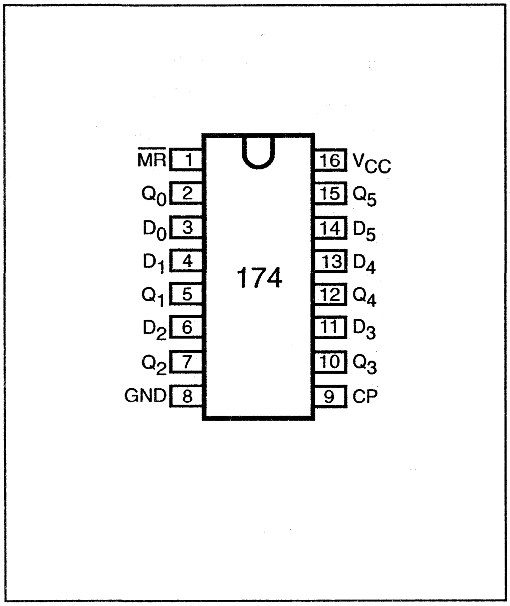

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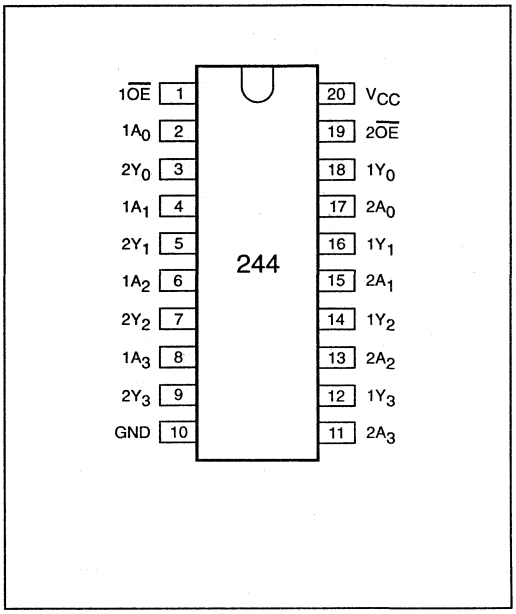

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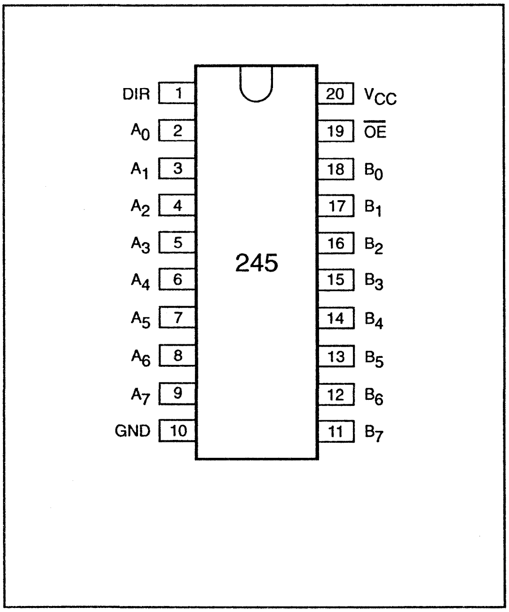

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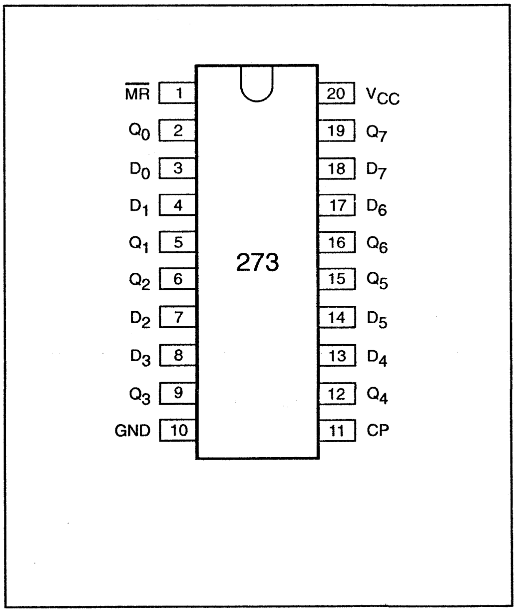

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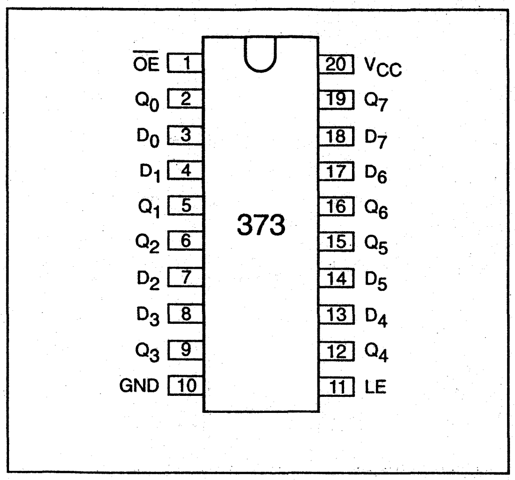

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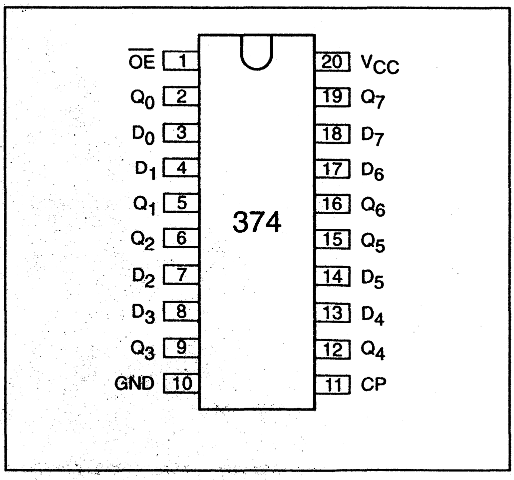

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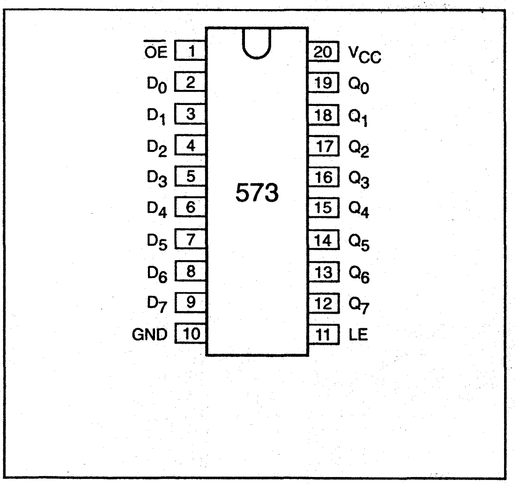

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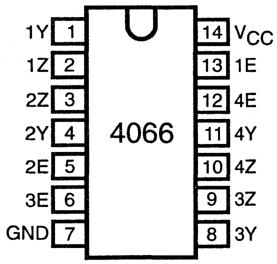
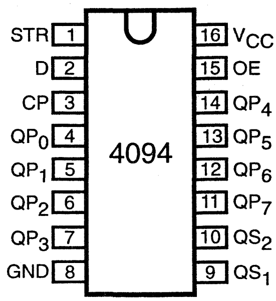


74LV4066



74LV4094

DEVICE DATA

HLL family

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**
- **5 V to 3.3 V level shifting**

DESCRIPTION

The 74HL33240 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74HL33240 is an octal inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.
The "240" is identical to the "244" but has inverting outputs.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	H
L	H	L
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 50 pF V_{CC} = 3.3 V	2.1	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33240D	24	SO	plastic	SO24/SOT137A
74HL33240DB	24	SSOP	plastic	SSOP24/SOT340

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4	$1Y_0$ to $1Y_3$	bus outputs
5, 6, 7, 8	GND	ground (0 V)
9, 10, 11, 12	$2Y_0$ to $2Y_3$	bus outputs
13	$2\overline{OE}$	output enable input (active LOW)
14, 15, 16, 17	$2A_3$ to $2A_0$	data inputs
18, 19	V_{CC}	positive supply voltage
20, 21, 22, 23	$1A_3$ to $1A_0$	data inputs
24	$1\overline{OE}$	output enable input (active LOW)

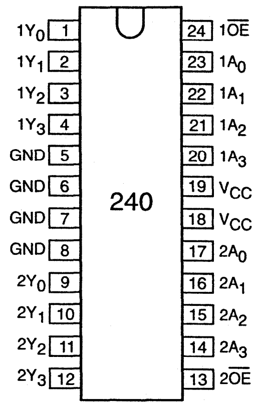


Fig.1 Pin configuration.

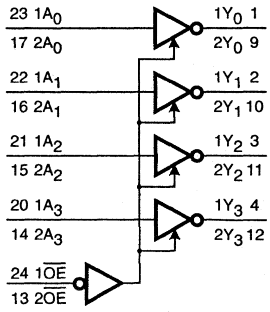


Fig.2 Logic symbol.

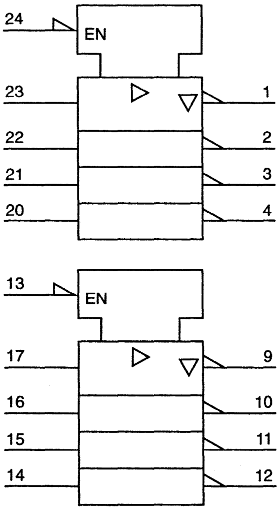


Fig.3 IEC logic symbol.

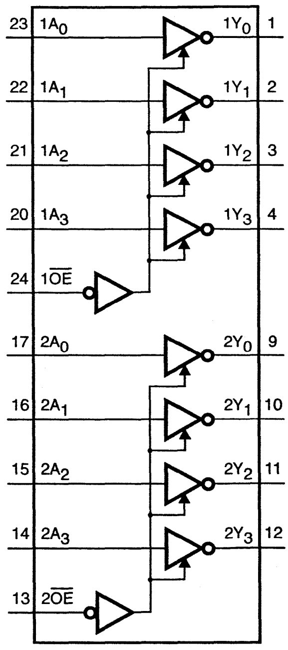


Fig.4 Functional diagram.

DC characteristics for 74HL33240

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".
I_{CC} category: MSI

AC characteristics for 74HL33240

GND = 0 V; $t_r = t_f = 2.0$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		-40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	- - -	14.0 5.3 3.5	- - -	16.0 6.0 4.0	ns	1.2 2.0 3.0	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$	- - -	15.6 5.9 3.9	- - -	17.6 6.6 4.4	ns	1.2 2.0 3.0	Fig. 6, 7
t_{PHZ}/t_{PLZ}	3-state output disable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$	- - -	12.3 5.4 4.0	- - -	13.9 6.0 4.4	ns	1.2 2.0 3.0	Fig. 6, 7

AC WAVEFORMS

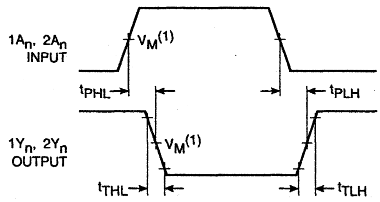


Fig. 5 Waveforms showing the input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays and the output transition times.

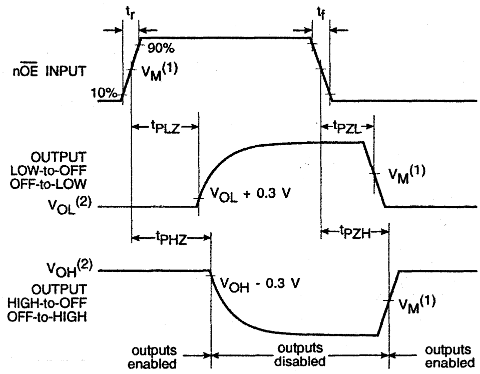


Fig.6 Waveforms showing the 3-state enable and disable times.

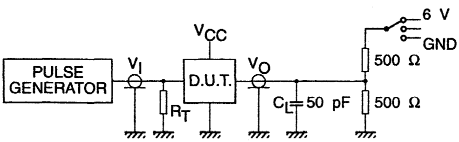


Fig. 7 Test conditions: Load circuitry for enable / disable times; switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**
- **5 V to 3.3 V level shifting**

DESCRIPTION

The 74HL33241 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74HL33241 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and 2OE.

FUNCTION TABLES

INPUTS		OUTPUT
$1\overline{OE}$	$1A_n$	$1Y_n$
L	L	L
L	H	H
H	X	Z

INPUTS		OUTPUT
2OE	$2A_n$	$2Y_n$
H	L	L
H	H	H
L	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF V_{CC} = 3.3 V	2.1	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33241D	24	SO	plastic	SO24/SOT137A
74HL33241DB	24	SSOP	plastic	SSOP24/SOT340

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4	$1Y_0$ to $1Y_3$	bus outputs
5, 6, 7, 8	GND	ground (0 V)
9, 10, 11, 12	$2Y_0$ to $2Y_3$	bus outputs
13	2OE	output enable input (active HIGH)
14, 15, 16, 17	$2A_3$ to $2A_0$	data inputs
18, 19	V_{CC}	positive power supply
20, 21, 22, 23	$1A_3$ to $1A_0$	data inputs
24	$1\overline{OE}$	output enable input (active LOW)

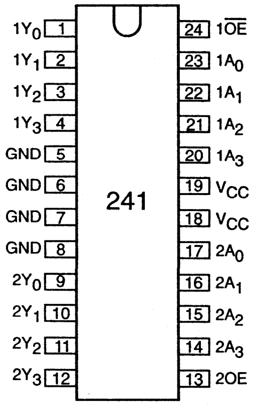


Fig.1 Pin configuration.

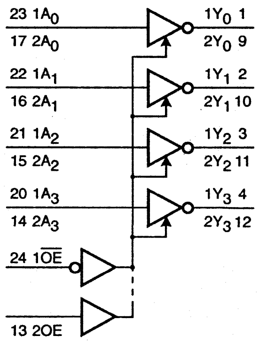


Fig.2 Logic symbol.

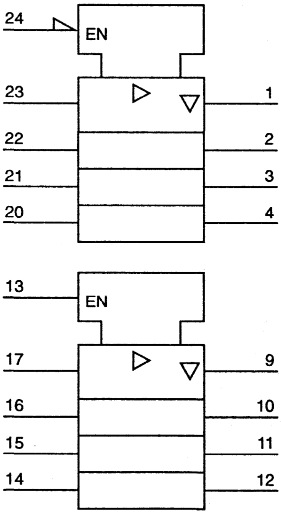


Fig.3 IEC logic symbol.

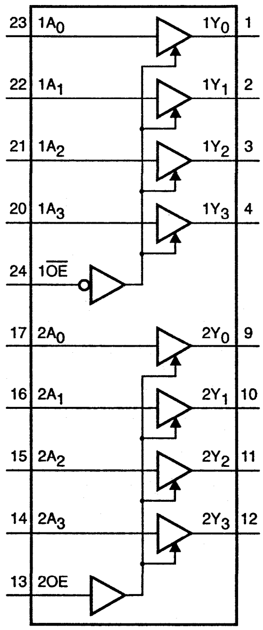


Fig.4 Functional diagram.

DC characteristics for 74HL33241

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

I_{CC} category: MSI

AC characteristics for 74HL33241

GND = 0 V; $t_r = t_f = 2.0$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		-40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	- - -	14.0 5.3 3.5	- - -	16.0 6.0 4.0	ns	1.2 2.0 3.0	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$	- - -	15.6 5.9 3.9	- - -	17.6 6.6 4.4	ns	1.2 2.0 3.0	Fig. 6, 8
t_{PHZ}/t_{PLZ}	3-state output disable time $1\overline{OE}$ to 1Yn	- - -	12.3 5.4 4.0	- - -	13.9 6.0 4.4	ns	1.2 2.0 3.0	Fig. 6. 8
t_{PZH}/t_{PZL}	3-state output enable time 2OE to $2Y_n$	- - -	15.6 5.9 3.9	- - -	17.6 6.6 4.4	ns	1.2 2.0 3.0	Fig. 7, 8
t_{PHZ}/t_{PLZ}	3-state output disable time 2OE to $2Y_n$	- - -	12.3 5.4 4.0	- - -	13.9 6.0 4.4	ns	1.2 2.0 3.0	Fig. 7, 8

AC WAVEFORMS

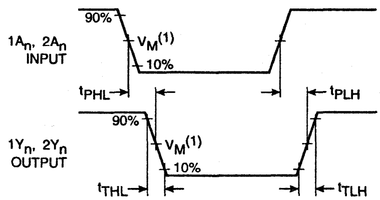


Fig. 5 Waveforms showing the input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays and the output transition times.

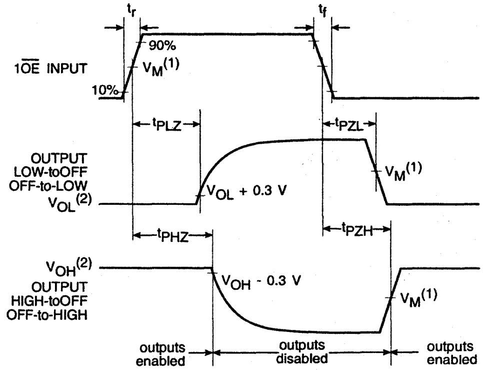


Fig.6 Waveforms showing the 3-state enable and disable times for input $1\overline{OE}$.

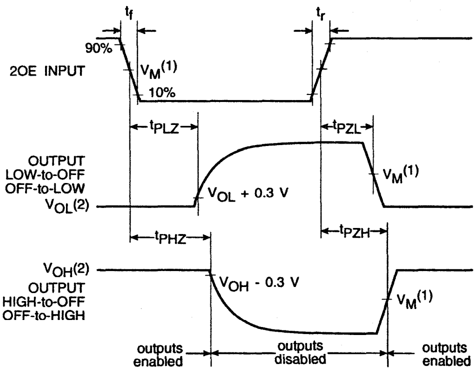


Fig.7 Waveforms showing the 3-state enable and disable times for input 2OE.

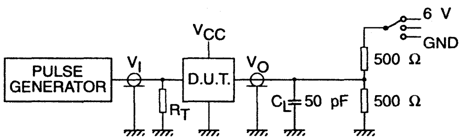


Fig. 8 Test conditions: Load circuitry for enable / disable times; switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**
- **5 V to 3.3 V level shifting**

DESCRIPTION

The 74HL33244 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74HL33244 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.
The "244" is identical to the "240" but has non-inverting outputs.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF V_{CC} = 3.3 V	2.1	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33244D	24	SO	plastic	SO24/SOT137A
74HL33244DB	24	SSOP	plastic	SSOP24/SOT340

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4	$1Y_0$ to $1Y_3$	bus outputs
5, 6, 7, 8	GND	ground (0 V)
9, 10, 11, 12	$2Y_0$ to $2Y_3$	bus outputs
13	$2\overline{OE}$	output enable input (active LOW)
14, 15, 16, 17	$2A_3$ to $2A_0$	data inputs
18, 19	V_{CC}	positive power supply
20, 21, 22, 23	$1A_3$ to $1A_0$	data inputs
24	$1\overline{OE}$	output enable input (active LOW)

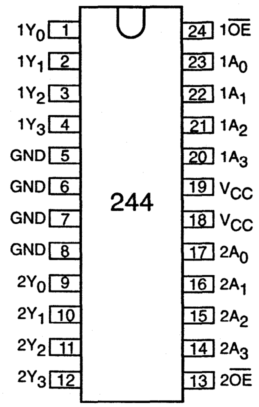


Fig.1 Pin configuration.

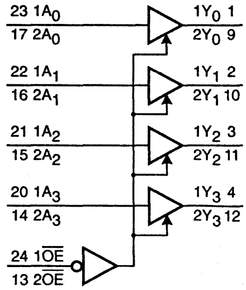


Fig.2 Logic symbol.

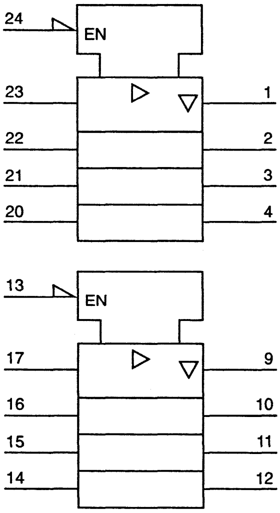


Fig.3 IEC logic symbol.

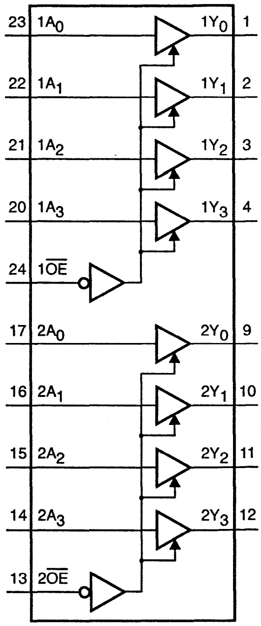


Fig.4 Functional diagram.

DC characteristics for 74HL33244

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

I_{CC} category: MSI

AC characteristics for 74HL33244

GND = 0 V; $t_r = t_f = 2.0$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		-40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	- - -	14.0 5.3 3.5	- - -	16.0 6.0 4.0	ns	1.2 2.0 3.0	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$	- - -	15.6 5.9 3.9	- - -	17.6 6.6 4.4	ns	1.2 2.0 3.0	Fig. 6, 7
t_{PHZ}/t_{PLZ}	3-state output disable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$	- - -	12.3 5.4 4.0	- - -	13.9 6.0 4.4	ns	1.2 2.0 3.0	Fig. 6, 7

AC WAVEFORMS

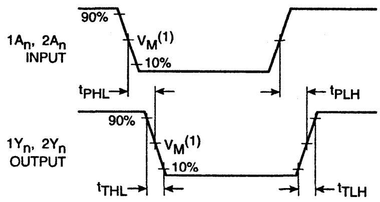


Fig. 5 Waveforms showing the input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays and the output transition times.

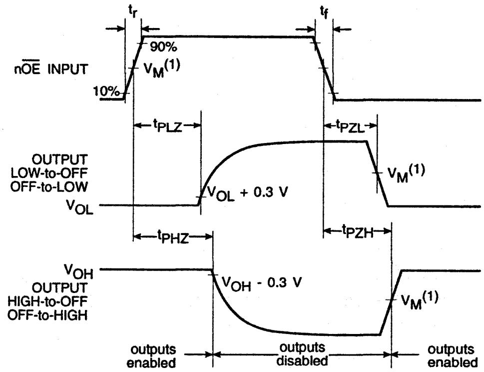


Fig.6 Waveforms showing the 3-state enable and disable times.

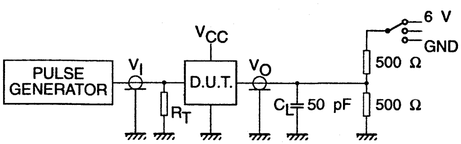


Fig. 8 Test conditions: Load circuitry for enable / disable times; switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Notes:

(1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with the JEDEC 3.3 V ±0.3 V supply
- CMOS low power consumption
- Flow-through pin-out architecture
- Low inductance, multiple centre power and ground pins for minimum noise and ground bounce
- Non-inverting 3-state outputs
- Direct interface with TTL levels

DESCRIPTION

The 74HL33245 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74HL33245 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The "245" features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.
The "245" is identical to the "640" but has true (non-inverting) outputs.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 50 pF V_{CC} = 3.3 V	2.2	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33245D	24	SO	plastic	SO24/SOT137A
74HL33245DB	24	SSOP	plastic	SSOP24/SOT340

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	A_0 to A_7	data inputs/outputs
5, 6, 7, 8	GND	ground (0 V)
13	$\overline{OE}$	output enable input (active LOW)
14, 15, 16, 17, 20, 21, 22, 23	B_7 to B_0	data inputs/outputs
18, 19	V_{CC}	positive supply voltage
24	DIR	direction control

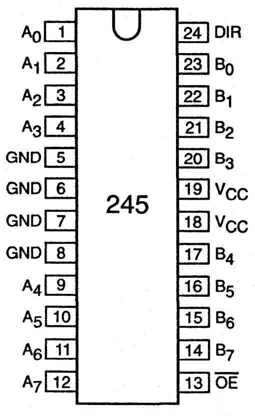


Fig.1 Pin configuration.

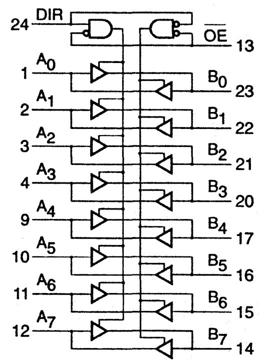


Fig.2 Logic symbol.

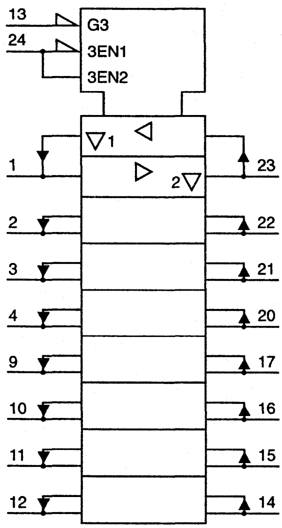


Fig.3 IEC logic symbol.

DC characteristics for 74HL33245

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".
I_{CC} category: MSI

AC characteristics for 74HL33245

GND = 0 V; $t_r = t_f = 2.0$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		-40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	- - -	14.0 5.3 3.5	- - -	16.0 6.0 4.0	ns	1.2 2.0 3.0	Fig. 4
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to A_n; $\overline{OE}$ to B_n	- - -	17.8 7.5 5.4	- - -	20.7 8.5 6.1	ns	1.2 2.0 3.0	Fig. 5, 6
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to A_n; $\overline{OE}$ to B_n	- - -	15.0 6.4 4.7	- - -	16.7 7.0 5.1	ns	1.2 2.0 3.0	Fig. 5, 6
t_{PZH}/t_{PZL}	3-state output enable time DIR to A_n; DIR to B_n	- - -	21.4 8.8 6.3	- - -	23.5 9.6 6.8	ns	1.2 2.0 3.0	Fig. 5, 6
t_{PHZ}/t_{PLZ}	3-state output disable time DIR to A_n; DIR to B_n	- - -	17.4 7.3 5.3	- - -	19.0 7.9 5.7	ns	1.2 2.0 3.0	Fig. 5, 6

AC WAVEFORMS

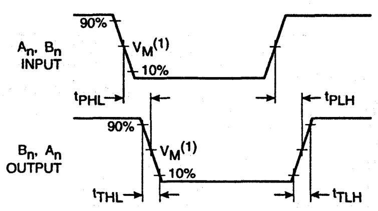


Fig. 4 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

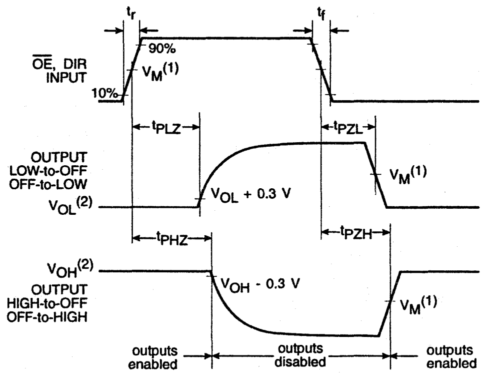


Fig.5 Waveforms showing the 3-state enable and disable times.

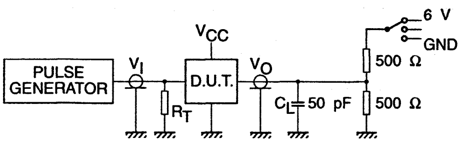


Fig. 6 Test conditions: Load circuitry for enable / disable times; switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Notes:

(1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**
- **5 V to 3.3 V level shifting**

DESCRIPTION

The 74HL33373 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) are common to all internal latches.

The "373" consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The "373" is functionally identical to the "533", but the "533" has inverted outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n; LE to Q_n	C_L = 50 pF V_{CC} = 3.3 V	 3.0 3.0	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	25	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33373D	24	SO	plastic	S024/SOT137A
74HL33373DB	24	SSOP	plastic	SSOP24/SOT340

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	Q_0 to Q_7	data outputs
5, 6, 7, 8	GND	ground (0 V)
13	LE	latch enable
23, 22, 21, 20, 17, 16, 15, 14	D_0 to D_7	data inputs
18, 19	V_{CC}	positive supply voltage
24	$\overline{OE}$	output enable input (active LOW)

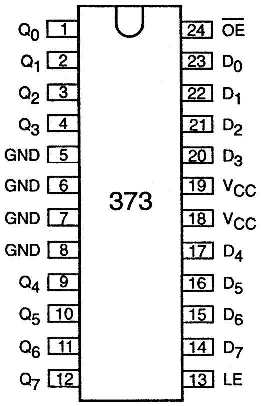


Fig.1 Pin configuration.

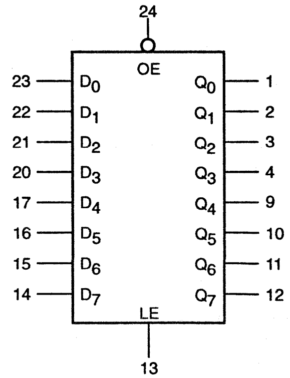


Fig.2 Logic symbol.

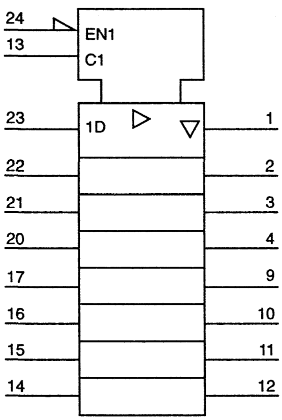


Fig3. IEC logic symbol.

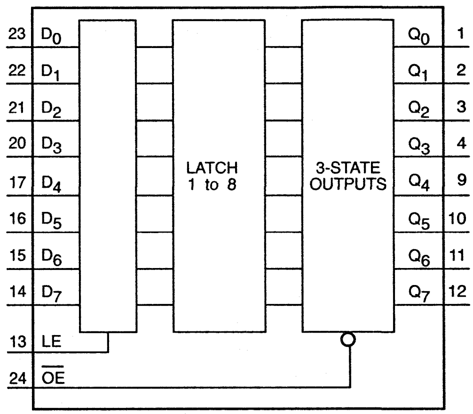


Fig.4 Functional diagram.

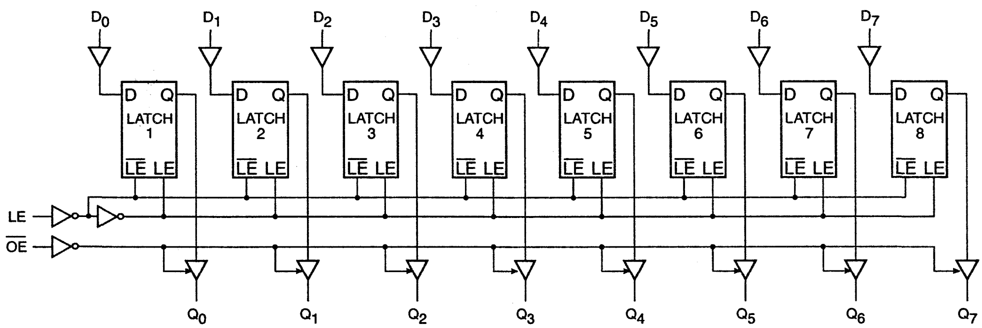


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{OE}$	LE	D_n	Q_0 to Q_7
enable and read register (transparent mode)	L L	H H	L H	L H
latch and read register	L L	L L	l h	L H
latch register and disable outputs	H	X	X	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state

DC characteristics for 74HL33373

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".
I_{CC} category: MSI

AC characteristics for 74HL33373

GND = 0 V; $t_r = t_f = 2.0$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		-40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n	– – –	16.0 6.0 4.0	– – –	17.6 6.6 4.4	ns	1.2 2.0 3.0	Fig.6
t_{PHL}/t_{PLH}	propagation delay LE to Q_n	– – –	17.6 6.6 4.4	– – –	19.2 7.2 4.8	ns	1.2 2.0 3.0	Fig.7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	– – –	18.4 6.9 4.6	– – –	20.0 7.5 5.0	ns	1.2 2.0 3.0	Fig.8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	– – –	18.8 7.0 4.7	– – –	20.2 7.6 5.1	ns	1.2 2.0 3.0	Fig.8
t_W	LE pulse width HIGH	3.0 2.0	– –	3.8 2.5	– –	ns	2.0 3.0	Fig.7
t_{su}	set-up time D_n to LE	2.0 0.8 0.5	– – –	2.2 0.9 0.6	– – –	ns	1.2 2.0 3.0	Fig.9
t_h	hold time D_n to LE	2.0 0.8 0.5	– – –	2.2 0.9 0.6	– – –	ns	1.2 2.0 3.0	Fig.9

AC WAVEFORMS

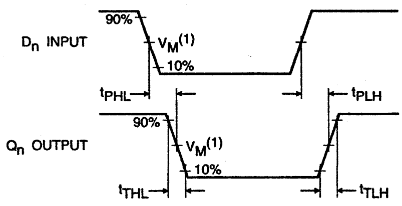


Fig.6 Waveforms showing the input (D_n) to output (Q_n) propagation delays and the output transition times.

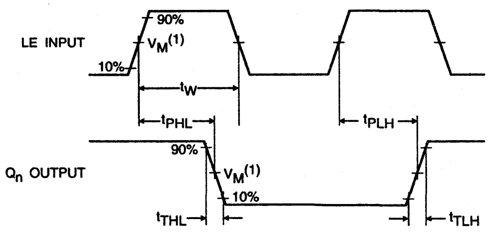


Fig.7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays and the output transition times.

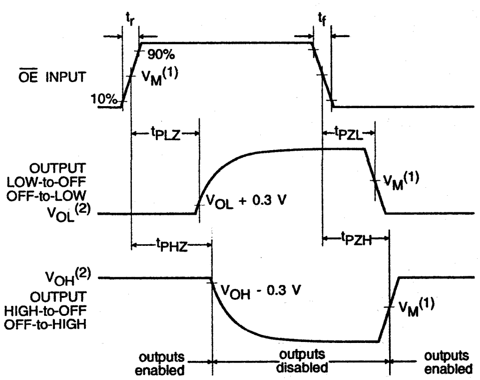


Fig.8 Waveforms showing the 3-state enable and disable times

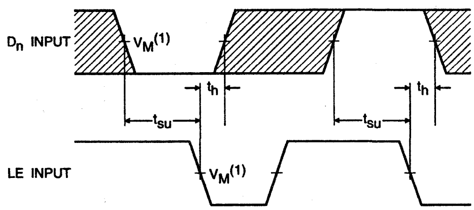


Fig.9 Waveforms showing the data set-up and hold times for th D_n input to the LE input.

Note to Fig.9:

The shaded areas indicate when the input is permitted to change for predictable output performance.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

Octal D-type flip-flop; positive edge-trigger; 3-state

74HL33374

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**
- **5 V to 3.3 V level shifting**

DESCRIPTION

The 74HL33374 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock (CP) input and an output enable ($\overline{OE}$) are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The "374" is functionally identical to the "534", but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 50 pF V_{CC} = 3.3 V	3.2	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	28	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33374D	24	SO	plastic	SO24/SOT137A
74HL33374DB	24	SSOP	plastic	SSOP24/SOT340

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	Q_0 to Q_7	data outputs
5, 6, 7, 8	GND	ground (0 V)
13	CP	clock input
23, 22, 21, 20, 17, 16, 15, 14	D_0 to D_7	data inputs
18, 19	V_{CC}	positive supply voltage
24	$\overline{OE}$	output enable input (active LOW)

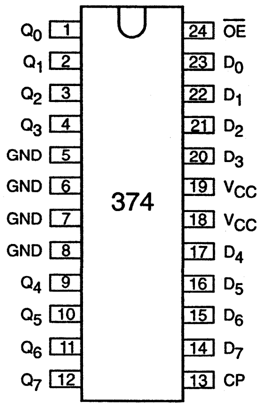


Fig.1 Pin configuration.

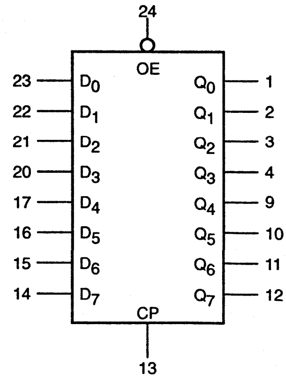


Fig.2 Logic symbol.

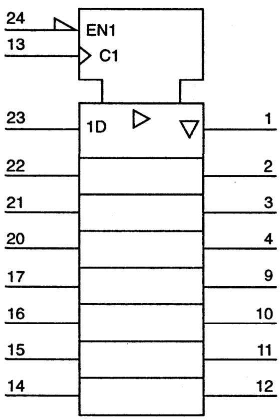


Fig3. IEC logic symbol.

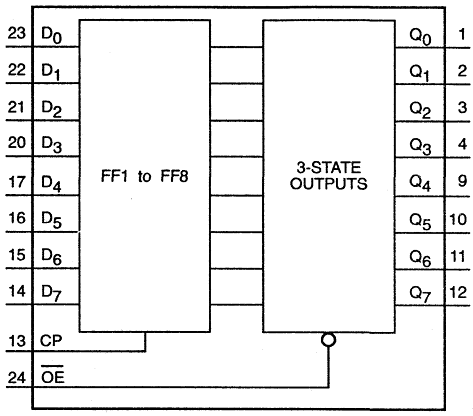


Fig.4 Functional diagram.

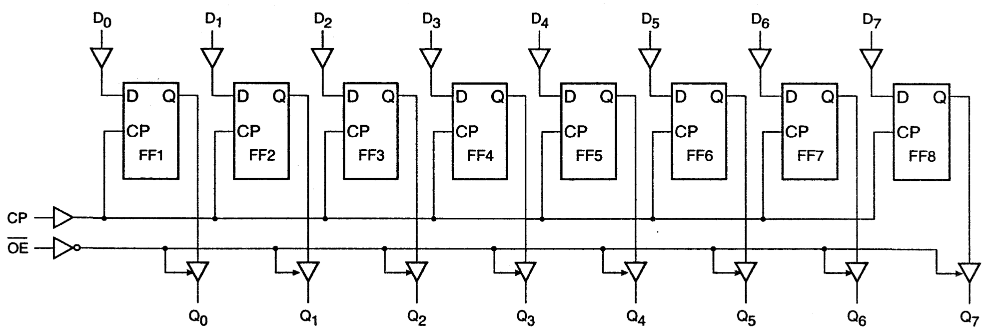


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{OE}$	CP	D_n	Q_0 to Q_7
load and read register	L L	↑ ↑	l h	L H
load register and disable outputs	H H	↑ ↑	l h	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH CP transition

DC characteristics for 74HL33374
For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".
I_{CC} category: MSI

AC characteristics for 74HL33374
GND = 0 V; t_r = t_f = 2.0 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		-40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	– – –	17.2 6.4 4.3	– – –	18.9 7.0 4.8	ns	1.2 2.0 3.0	Fig.6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	– – –	18.4 6.9 4.6	– – –	20.0 7.5 5.0	ns	1.2 2.0 3.0	Fig.7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	– – –	18.8 7.0 4.7	– – –	20.2 7.6 5.1	ns	1.2 2.0 3.0	Fig.7
t_W	CP pulse width HIGH or LOW	3.0 2.0	– –	3.8 2.5	– –	ns	2.0 3.0	Fig.6
t_{su}	set-up time D_n to CP	2.0 0.8 0.5	– – –	2.2 0.9 0.6	– – –	ns	1.2 2.0 3.0	Fig.8
t_h	hold time D_n to CP	2.0 0.8 0.5	– – –	2.2 0.9 0.6	– – –	ns	1.2 2.0 3.0	Fig.8
f_{max}	maximum clock pulse frequency	166 250	– –	135 200	– –	MHz	2.0 3.0	Fig.6

AC WAVEFORMS

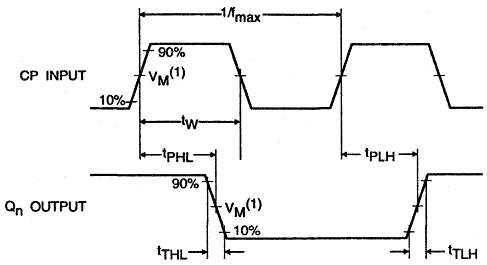


Fig.6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

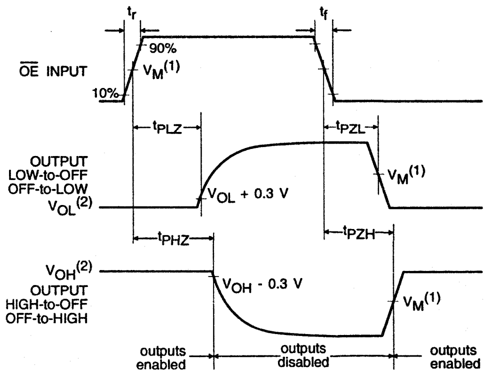


Fig.7 Waveforms showing the 3-state enable and disable times.

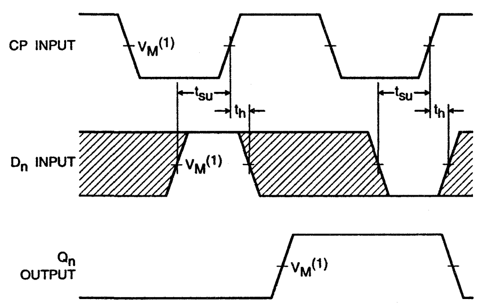


Fig.8 Waveforms showing the data set-up and hold times for th D_n input.

Note to Fig.8:

The shaded areas indicate when the input is permitted to change for predictable output performance.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

Octal D-type transparent latch; 3-state; inverting

74HL33533

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**
- **5 V to 3.3 V level shifting**

DESCRIPTION

The 74HL33533 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) are common to all internal latches.

The "533" consists of eight D-type transparent latches with 3-state inverting outputs. When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The "533" is functionally identical to the "373", but the "373" has non-inverted outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay D_n to $\overline{Q}_n$; LE to $\overline{Q}_n$	C_L = 50 pF V_{CC} = 3.3 V	3.0 3.0	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	25	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33533D	24	SO	plastic	SO24/SOT137A
74HL33533DB	24	SSOP	plastic	SSOP24/SOT340

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	$\overline{Q}_0$ to $\overline{Q}_7$	data outputs
5, 6, 7, 8	GND	ground (0 V)
13	LE	latch enable
23, 22, 21, 20, 17, 16, 15, 14	D_0 to D_7	data inputs
18, 19	V_{CC}	positive supply voltage
24	$\overline{OE}$	output enable input (active LOW)

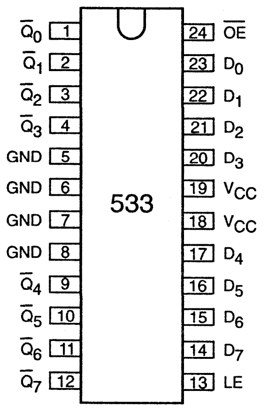


Fig.1 Pin configuration.

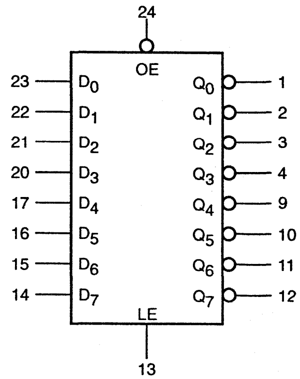


Fig.2 Logic symbol.

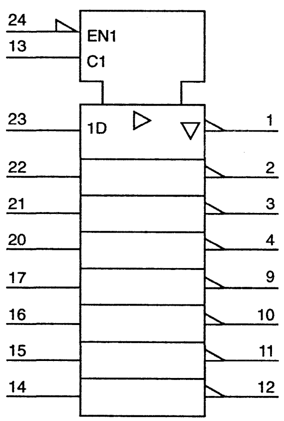


Fig.3 IEC logic symbol.

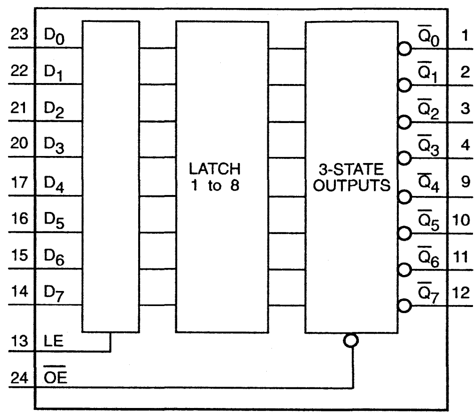


Fig.4 Functional diagram.

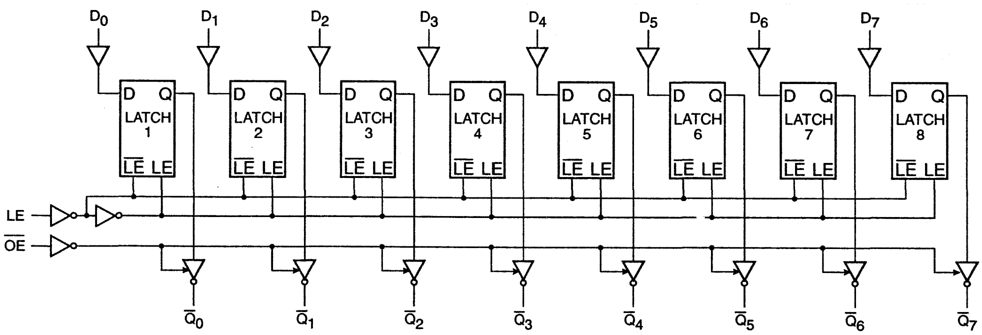


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{OE}$	LE	D_n	$\overline{Q}_0$ to $\overline{Q}_7$
enable and read register (transparent mode)	L L	H H	L H	H L
latch and read register	L L	L L	l h	H L
latch register and disable outputs	H	X	X	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state

DC characteristics for 74HL33533

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".
I_{CC} category: MSI

AC characteristics for 74HL33533

GND = 0 V; $t_r = t_f = 2.0$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		-40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay D_n to $\overline{Q}_n$	– – –	16.0 6.0 4.0	– – –	17.6 6.6 4.4	ns	1.2 2.0 3.0	Fig.6
t_{PHL}/t_{PLH}	propagation delay LE to $\overline{Q}_n$	– – –	17.6 6.6 4.4	– – –	19.2 7.2 4.8	ns	1.2 2.0 3.0	Fig.7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$	– – –	18.4 6.9 4.6	– – –	20.0 7.5 5.0	ns	1.2 2.0 3.0	Fig.8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$	– – –	18.8 7.0 4.7	– – –	20.2 7.6 5.1	ns	1.2 2.0 3.0	Fig.8
t_W	LE pulse width HIGH	3.0 2.0	– –	3.8 2.5	– –	ns	2.0 3.0	Fig.7
t_{su}	set-up time D_n to LE	2.0 0.8 0.5	– – –	2.2 0.9 0.6	– – –	ns	1.2 2.0 3.0	Fig.9
t_h	hold time D_n to LE	2.0 0.8 0.5	– – –	2.2 0.9 0.6	– – –	ns	1.2 2.0 3.0	Fig.9

AC WAVEFORMS

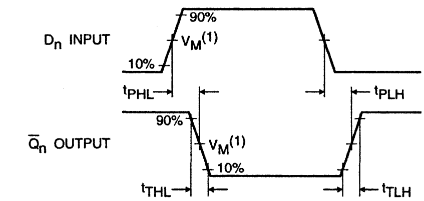


Fig.6 Waveforms showing the input (D_n) to output ($\overline{Q}_n$) propagation delays and the output transition times.

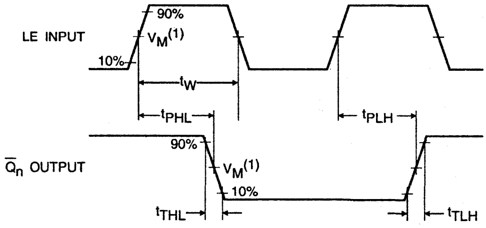


Fig.7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output ($\overline{Q}_n$) propagation delays and the output transition times.

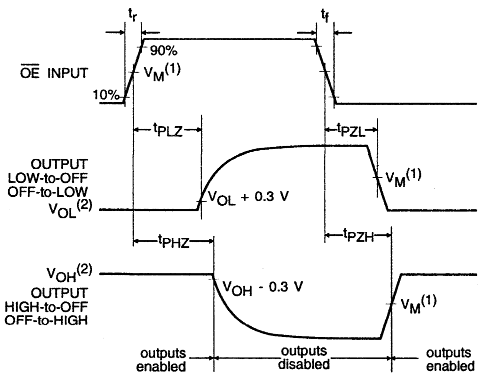


Fig.8 Waveforms showing the 3-state enable and disable times

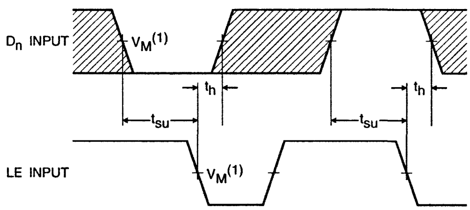


Fig.9 Waveforms showing the data set-up and hold times for th D_n input to the LE input.

Note to Fig.9:

The shaded areas indicate when the input is permitted to change for predictable output performance.

Notes: (1) $V_M = 0.6$ V at $V_{CC} = 1.2$ V.
$V_M = 1.0$ V at $V_{CC} = 2.0$ V.
$V_M = 1.5$ V at $V_{CC} = 3.0$ V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

Octal D-type flip-flop; positive edge-trigger; 3-state;inverting

74HL33534

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state inverting outputs**
- **Direct interface with TTL levels**
- **5 V to 3.3 V level shifting**

DESCRIPTION

The 74HL33534 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock (CP) input and an output enable ($\overline{OE}$) are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The "534" is functionally identical to the "374", but has inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{Q}_n$	C_L = 50 pF V_{CC} = 3.3 V	3.2	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	28	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33534D	24	SO	plastic	SO24/SOT137A
74HL33534DB	24	SSOP	plastic	SSOP24/SOT340

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	$\overline{Q}_0$ to $\overline{Q}_7$	data outputs
5, 6, 7, 8	GND	ground (0 V)
13	CP	clock input
23, 22, 21, 20, 17, 16, 15, 14	D_0 to D_7	data inputs
18, 19	V_{CC}	positive supply voltage
24	$\overline{OE}$	output enable input (active LOW)

Octal D-type flip-flop; positive edge-trigger; 3-state;inverting

74HL33534

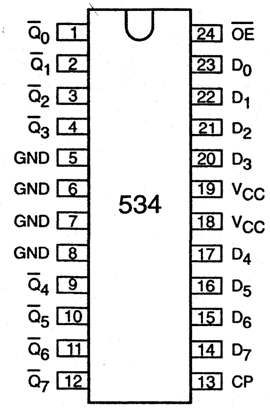


Fig.1 Pin configuration.

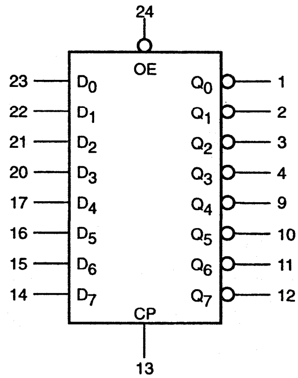


Fig.2 Logic symbol.

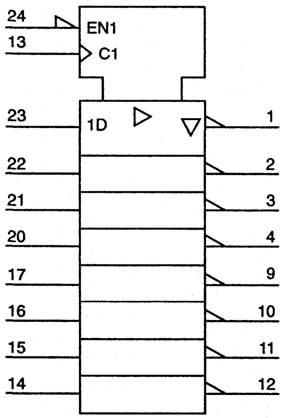


Fig.3 IEC logic symbol.

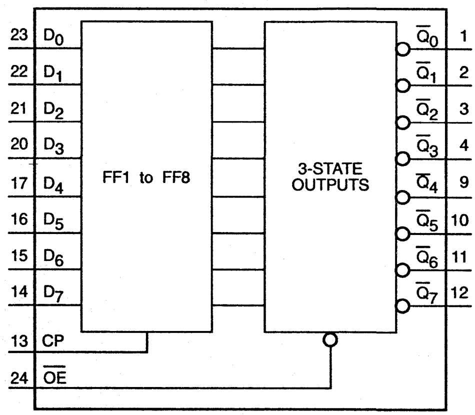


Fig.4 Functional diagram.

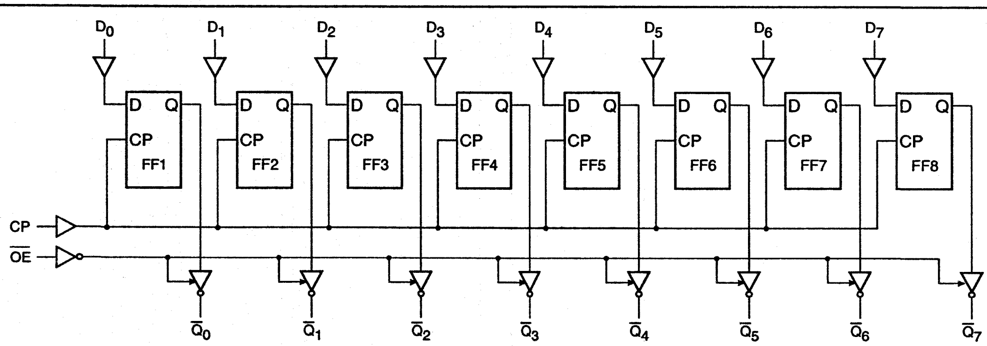


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{OE}$	CP	D_n	$\overline{Q}_0$ to $\overline{Q}_7$
load and read register	L L	↑ ↑	l h	H L
load register and disable outputs	H H	↑ ↑	l h	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
Z = high impedance OFF-state
↑ = LOW-to-HIGH CP transition

DC characteristics for 74HL33534

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".
I_{CC} category: MSI

AC characteristics for 74HL33534

GND = 0 V; $t_r = t_f = 2.0$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		-40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to $\overline{Q}_n$	– – –	17.2 6.4 4.3	– – –	18.9 7.0 4.8	ns	1.2 2.0 3.0	Fig.6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$	– – –	18.4 6.9 4.6	– – –	20.0 7.5 5.0	ns	1.2 2.0 3.0	Fig.7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$	– – –	18.8 7.0 4.7	– – –	20.2 7.6 5.1	ns	1.2 2.0 3.0	Fig.7
t_W	CP pulse width HIGH or LOW	3.0 2.0	– –	3.8 2.5	– –	ns	2.0 3.0	Fig.6
t_{su}	set-up time D_n to CP	2.0 0.8 0.5	– – –	2.2 0.9 0.6	– – –	ns	1.2 2.0 3.0	Fig.8
t_h	hold time D_n to CP	2.0 0.8 0.5	– – –	2.2 0.9 0.6	– – –	ns	1.2 2.0 3.0	Fig.8
f_{max}	maximum clock pulse frequency	166 250	– –	135 200	– –	MHz	2.0 3.0	Fig.6

AC WAVEFORMS

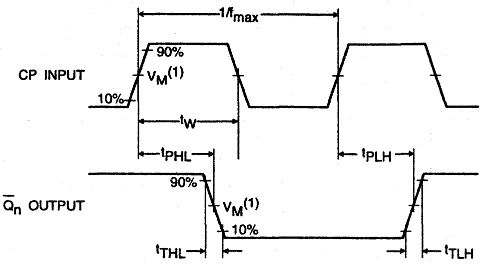


Fig.6 Waveforms showing the clock (CP) to output ($\overline{Q}_n$) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

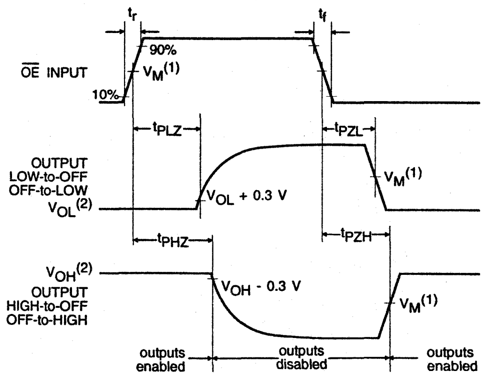


Fig.7 Waveforms showing the 3-state enable and disable times.

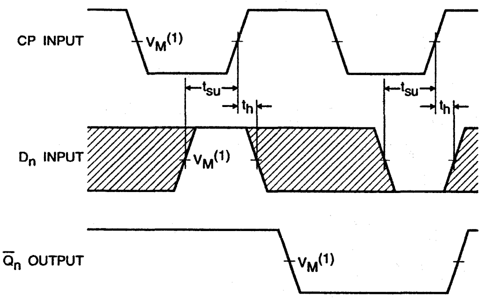


Fig.8 Waveforms showing the data set-up and hold times for th D_n input.

Note to Fig.8:

The shaded areas indicate when the input is permitted to change for predictable output performance.

Notes:

(1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **Inverting 3-state outputs**
- **Direct interface with TTL levels**

DESCRIPTION

The 74HL33620 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74HL33620 is an octal transceiver featuring inverting 3-state bus compatible outputs in both send and receive directions.

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The control function implementation allows maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs (OE_{AB}, $\overline{OE}_{BA}$). The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual enable function configuration gives this transceiver the capability to store data by simultaneous enabling of OE_{AB} and $\overline{OE}_{BA}$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance OFF-state, both sets of bus lines will remain at their last states.The 8-bit codes appearing on the two sets of buses will be complementary.
The "620" is identical to the "623" but has inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 50 pF V_{CC} = 3.3 V	2.2	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33620D	24	SO	plastic	SO24/SOT137A
74HL33620DB	24	SSOP	plastic	SSOP24/SOT340

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	A_0 to A_7	data inputs/outputs
5, 6, 7, 8	GND	ground (0 V)
13	$\overline{OE}_{BA}$	output enable input (active LOW)
14, 15, 16, 17, 20, 21, 22, 23	B_7 to B_0	data inputs/outputs
18, 19	V_{CC}	positive supply voltage
24	OE_{AB}	output enable input (active HIGH)

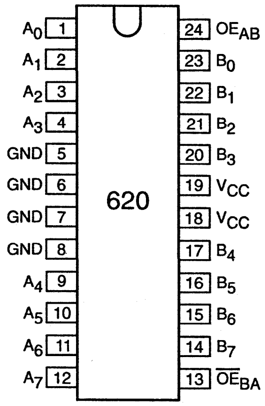


Fig.1 Pin configuration.

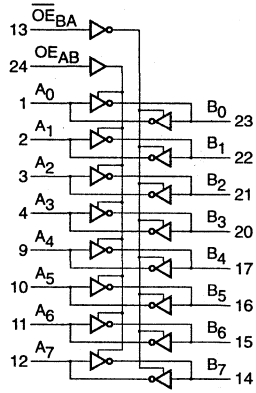


Fig.2 Logic symbol.

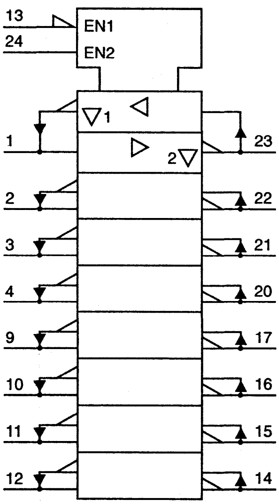


Fig.3 IEC logic symbol.

FUNCTION TABLE

ENABLE INPUTS		OPERATION
OE_{AB}	$\overline{OE}_{BA}$	
L	L	$\overline{B}$ data to A bus
H	H	$\overline{A}$ data to B bus
L	H	Z
H	L	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state

DC characteristics for 74HL33620

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

I_{CC} category: MSI

AC characteristics for 74HL33620

GND = 0 V; $t_r = t_f = 2.0$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		-40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	- - -	14.0 5.3 3.5	- - -	16.0 6.0 4.0	ns	1.2 2.0 3.0	Fig. 4
t_{PZH}/t_{PZL}	3-state output enable time OE_{AB} to B_n	- - -	13.1 5.7 4.2	- - -	14.3 6.1 4.5	ns	1.2 2.0 3.0	Fig. 5, 6
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{AB} to B_n	- - -	14.3 6.1 4.5	- - -	15.5 6.6 4.8	ns	1.2 2.0 3.0	Fig. 5, 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to A_n	- - -	12.3 5.4 4.0	- - -	13.5 5.8 4.3	ns	1.2 2.0 3.0	Fig. 5, 6
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$ to A_n	- - -	12.3 5.4 4.0	- - -	13.9 6.0 4.3	ns	1.2 2.0 3.0	Fig. 5, 6

AC WAVEFORMS

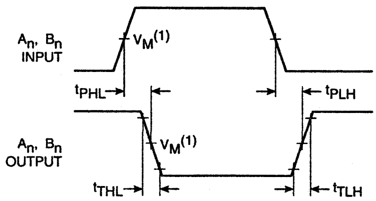


Fig. 4 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

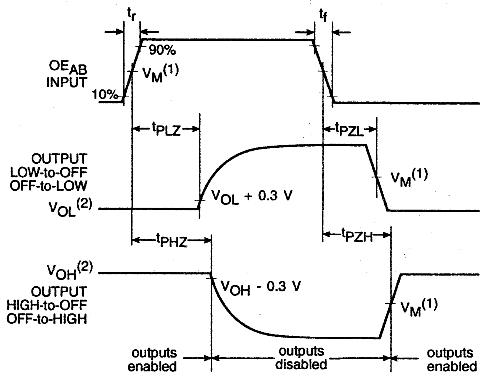


Fig.5 Waveforms showing the 3-state enable and disable times for OE_{AB} input.

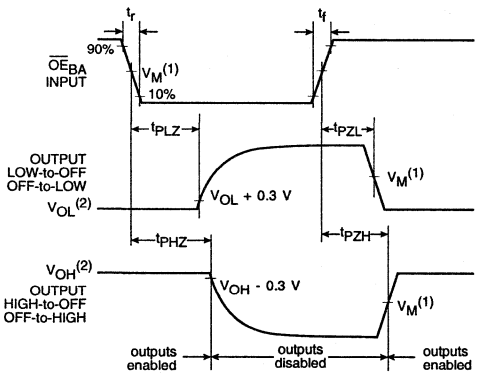


Fig.6 Waveforms showing the 3-state enable and disable times for $\overline{OE}_{AB}$ input.

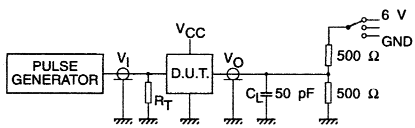


Fig. 7 Test conditions: Load circuitry for enable / disable times; switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Notes:

(1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **Non-inverting 3-state outputs**
- **Direct interface with TTL levels**

DESCRIPTION

The 74HL33623 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74HL33623 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions.

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The control function implementation allows maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs (OE_{AB}, $\overline{OE}_{BA}$). The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual enable function configuration gives this transceiver the capability to store data by simultaneous enabling of OE_{AB} and $\overline{OE}_{BA}$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance OFF-state, both sets of bus lines will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical.
The "623" is identical to the "620" but has true (non-inverting) outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 50 pF V_{CC} = 3.3 V	2.2	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33623D	24	SO	plastic	SO24/SOT137A
74HL33623DB	24	SSOP	plastic	SSOP24/SOT340

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	A_0 to A_7	data inputs/outputs
5, 6, 7, 8	GND	ground (0 V)
13	$\overline{OE}_{BA}$	output enable input (active LOW)
14, 15, 16, 17, 20, 21, 22, 23	B_7 to B_0	data inputs/outputs
18, 19	V_{CC}	positive supply voltage
24	OE_{AB}	output enable input (active HIGH)

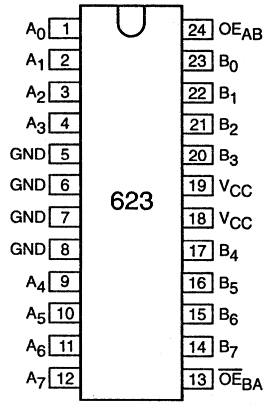


Fig.1 Pin configuration.

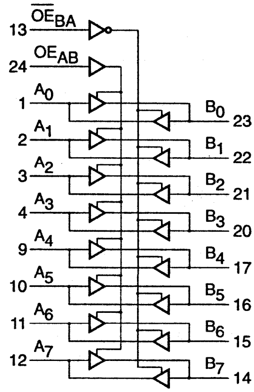


Fig.2 Logic symbol.

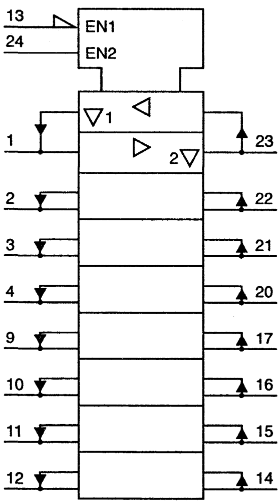


Fig.3 IEC logic symbol.

FUNCTION TABLE

ENABLE INPUTS		OPERATION
OE_{AB}	$\overline{OE}_{BA}$	
L	L	B data to A bus
H	H	A data to B bus
L	H	Z
H	L	B data to A bus, A data to B bus

H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state

DC characteristics for 74HL33623

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

I_{CC} category: MSI

AC characteristics for 74HL33623

GND = 0 V; $t_r = t_f = 2.0$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		-40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	- - -	14.0 5.3 3.5	- - -	16.0 6.0 4.0	ns	1.2 2.0 3.0	Fig. 4
t_{PZH}/t_{PZL}	3-state output enable time OE_{AB} to B_n	- - -	13.1 5.7 4.2	- - -	14.3 6.1 4.5	ns	1.2 2.0 3.0	Fig. 5, 6
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{AB} to B_n	- - -	14.3 6.1 4.5	- - -	15.5 6.6 4.8	ns	1.2 2.0 3.0	Fig. 5, 6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to A_n	- - -	12.3 5.4 4.0	- - -	13.5 5.8 4.3	ns	1.2 2.0 3.0	Fig. 5, 6
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$ to A_n	- - -	12.3 5.4 4.0	- - -	13.9 6.0 4.3	ns	1.2 2.0 3.0	Fig. 5, 6

AC WAVEFORMS

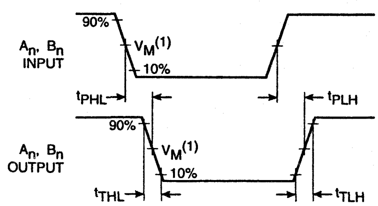


Fig. 4 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

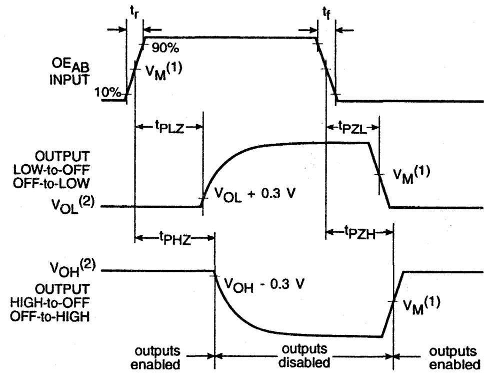


Fig.5 Waveforms showing the 3-state enable and disable times for OE_{AB} input.

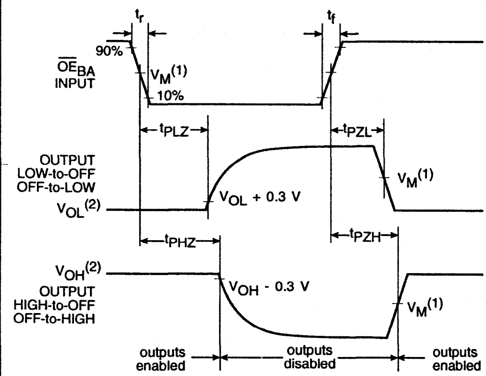


Fig.6 Waveforms showing the 3-state enable and disable times for $\overline{OE}_{BA}$ input.

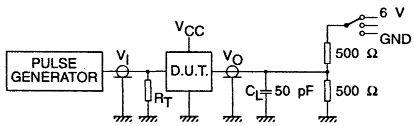


Fig.7 Test conditions: Load circuitry for enable / disable times; switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Notes:

(1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **Inverting 3-state outputs**
- **Direct interface with TTL levels**

DESCRIPTION

The 74HL33640 is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74HL33640 is an octal transceiver featuring inverting 3-state bus compatible outputs in both send and receive directions. The "640" features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.
The "640" is identical to the "245" but has inverting outputs.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
$\overline{OE}$	DIR	A_n	B_n
L	L	$A = \overline{B}$	inputs
L	H	inputs	$B = \overline{A}$
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 50 pF V_{CC} = 3.3 V	2.2	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33640D	24	SO	plastic	SO24/SOT137A
74HL33640DB	24	SSOP	plastic	SSOP24/SOT340

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 9, 10, 11, 12	A_0 to A_7	data inputs/outputs
5, 6, 7, 8	GND	ground (0 V)
13	$\overline{OE}$	output enable input (active LOW)
14, 15, 16, 17, 20, 21, 22, 23	B_7 to B_0	data inputs/outputs
18, 19	V_{CC}	positive supply voltage
24	DIR	direction control

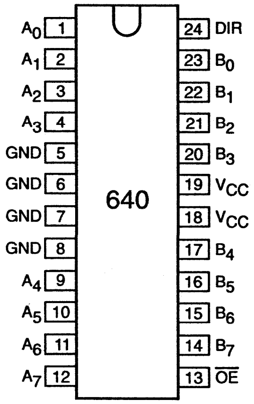


Fig.1 Pin configuration.

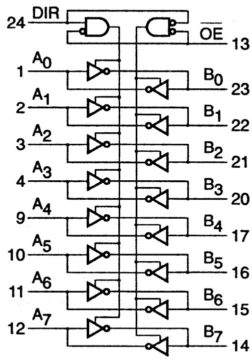


Fig.2 Logic symbol.

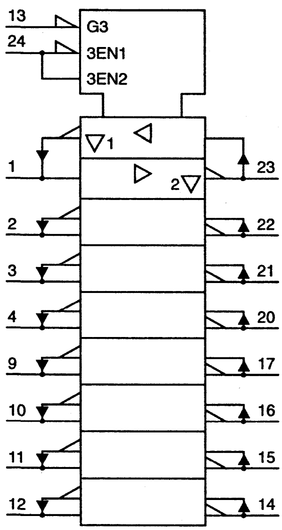


Fig.3 IEC logic symbol.

DC characteristics for 74HL33640

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

I_{CC} category: MSI

AC characteristics for 74HL33640

GND = 0 V; t_r = t_f = 2.0 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		-40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	- - -	14.0 5.3 3.5	- - -	16.0 6.0 4.0	ns	1.2 2.0 3.0	Fig. 4
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to A_n; $\overline{OE}$ to B_n	- - -	17.8 7.5 5.4	- - -	20.7 8.5 6.1	ns	1.2 2.0 3.0	Fig. 5, 6
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to A_n; $\overline{OE}$ to B_n	- - -	15.0 6.4 4.7	- - -	16.7 7.0 5.1	ns	1.2 2.0 3.0	Fig. 5, 6
t_{PZH}/t_{PZL}	3-state output enable time DIR to A_n; DIR to B_n	- - -	21.4 8.8 6.3	- - -	23.5 9.6 6.8	ns	1.2 2.0 3.0	Fig. 5, 6
t_{PHZ}/t_{PLZ}	3-state output disable time DIR to A_n; DIR to B_n	- - -	17.4 7.3 5.3	- - -	19.0 7.9 5.7	ns	1.2 2.0 3.0	Fig. 5, 6

AC WAVEFORMS

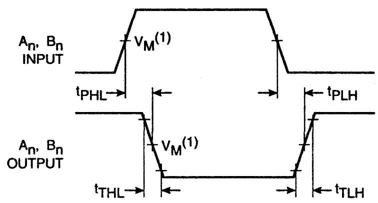


Fig. 4 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

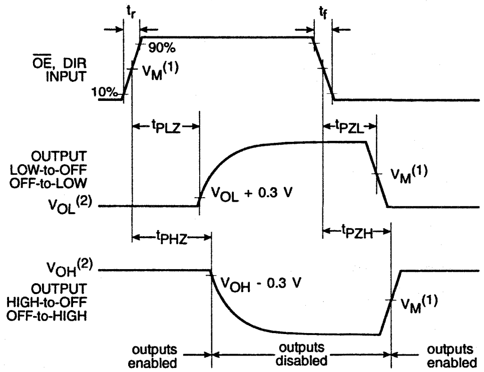


Fig.5 Waveforms showing the 3-state enable and disable times.

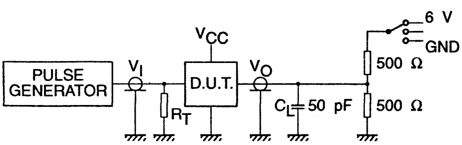


Fig. 6 Test conditions: Load circuitry for enable / disable times; switch set to 6 V for t_{PLZ}/t_{PZL}, switch set to GND for t_{PHZ}/t_{PZH} otherwise do not connect.

Notes:

(1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**

DESCRIPTION

The 74HL33646 consist of 8 non-inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the 'A' or 'B' bus will be clocked in the internal registers, as the appropiate clock (CP_{AB} or CP_{BA}) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the 'A' or 'B' register, or in both.The select source inputs (S_{AB} and S_{BA}) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when $\overline{OE}$ is active (LOW). In the isolation mode ($\overline{OE}$ = HIGH), 'A' data may be stored in the 'B' register and/or 'B' data may be stored in the 'A' register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, 'A' or 'B' may be driven at a time.

The '646' is functionally identical to the '648', but has non-inverting data paths.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	C_L = 50 pF V_{CC} = 3.3 V	3.2	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33646D	28	SO	plastic	SO28/SOT136A
74HL33646DB	28	SSOP	plastic	SSOP28/SOT341

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 3, 4, 5, 10, 11, 12, 13	A_0 to A_7	'A' data inputs/outputs
6, 7, 8, 9	GND	ground (0 V)
14	DIR	direction control input
15	S_{BA}	select 'B' to 'A' source input
16	CP_{BA}	'B' to 'A' clock input (Low-to-High, edge-triggered)
26, 25, 24, 23, 20, 19, 18, 17	B_0 to B_7	'B' data inputs/outputs
21, 22	V_{CC}	positive supply voltage
27	S_{AB}	select 'A' to 'B' source input
28	CP_{AB}	'A' to 'B' clock input (Low-to-High, edge-triggered)

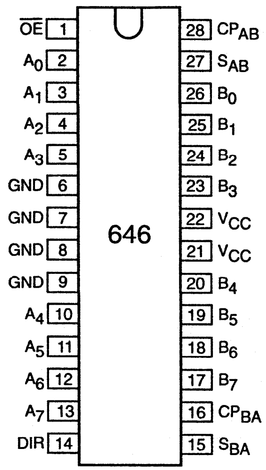


Fig.1 Pin configuration.

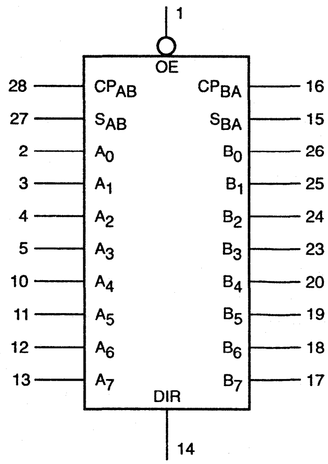


Fig.2 Logic symbol.

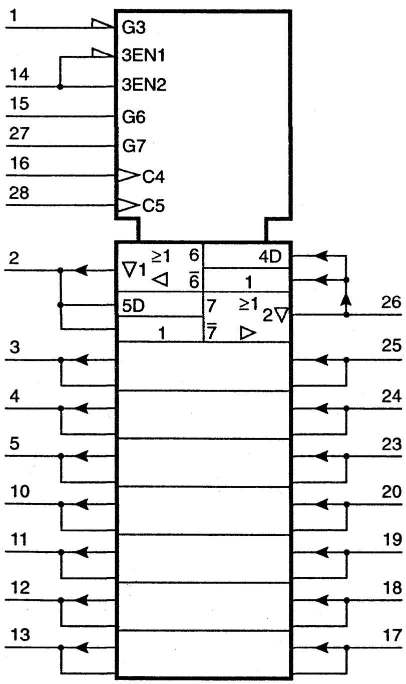


Fig3. IEC logic symbol.

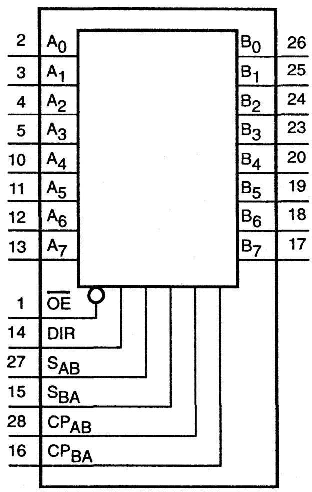


Fig.4 Functional diagram.

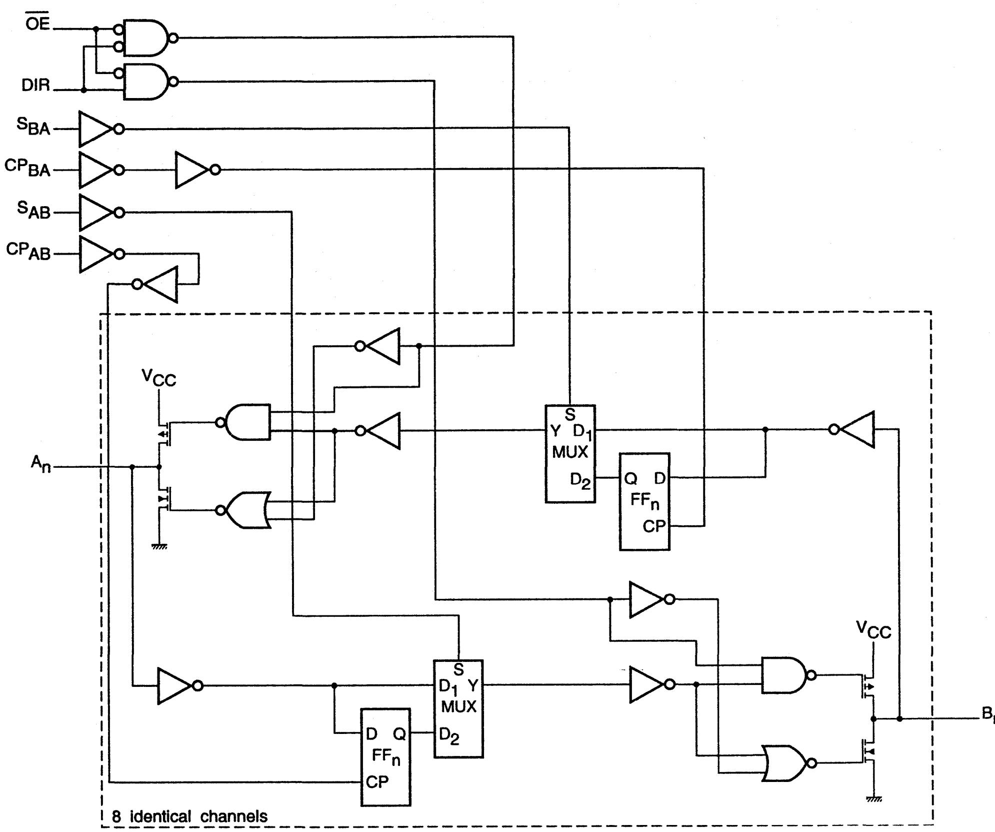


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_0 to A_7	B_0 to B_7	
X X	X X	↑ X	X ↑	X X	X X	input un*	un* input	store A, B unspecified* store B, A unspecified*
H H	X X	↑ H or L	↑ H or L	X X	X X	input	input	store A and B data, isolation hold storage
L L	L L	X X	X H or L	X X	L H	output	input	real-time B data to A bus stored B data to A bus
L L	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus

* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

DC characteristics for 74HL33646

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

I_{CC} category: MSI

AC characteristics for 74HL33646

GND = 0 V; $t_r = t_f$ = 2.0 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) +25 MIN.	+25 MAX.	-40 to +85 MIN.	-40 to +85 MAX.	UNIT	TEST CONDITIONS V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	– – –	18.0 6.8 4.5	– – –	20.8 7.8 5.2	ns	1.2 2.0 3.0	Fig.6
t_{PHL}/t_{PLH}	propagation delay CP_{AB}, CP_{BA} to B_n, A_n	– – –	22.8 8.6 5.7	– – –	26.4 9.9 6.6	ns	1.2 2.0 3.0	Fig.7
t_{PHL}/t_{PLH}	propagation delay S_{AB}, S_{BA} to B_n, A_n	– – –	23.2 8.6 5.8	– – –	26.8 10.1 6.7	ns	1.2 2.0 3.0	Fig.8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to A_n, B_n	– – –	17.8 7.5 5.4	– – –	20.7 8.5 6.5	ns	1.2 2.0 3.0	Fig.9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to A_n, B_n	– – –	15.0 6.4 4.7	– – –	16.7 7.0 5.1	ns	1.2 2.0 3.0	Fig.9
t_{PZH}/t_{PZL}	3-state output enable time DIR to A_n, B_n	– – –	21.4 8.8 6.3	– – –	23.5 9.6 6.8	ns	1.2 2.0 3.0	Fig.10
t_{PHZ}/t_{PLZ}	3-state output disable time DIR to A_n, B_n	– – –	17.4 7.3 5.3	– – –	19.0 7.9 5.7	ns	1.2 2.0 3.0	Fig.10
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	3.0 3.0	– –	3.7 2.5	– –	ns	2.0 3.0	Figs 6 and 8
t_{su}	set-up time A_n, B_n to CP_{AB}, CP_{BA}	 0.5	– – –	 0.5	– – –	ns	1.2 2.0 3.0	Fig.7
t_h	hold time A_n, B_n to CP_{AB}, CP_{BA}	 0.5	– – –	 0.5	– – –	ns	1.2 2.0 3.0	Fig.7
f_{max}	maximum clock pulse frequency	166 250	– –	135 200	– –	ns	2.0 3.0	Fig.7

AC WAVEFORMS

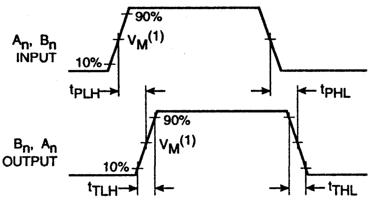


Fig.6 Waveforms showing the input A_n, B_n to output B_n, A_n propagation delays and the output transition times.

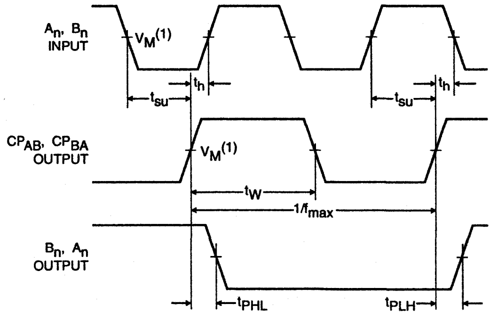


Fig.7 Waveforms showing the A_n, B_n to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output B_n, A_n propagation delays.

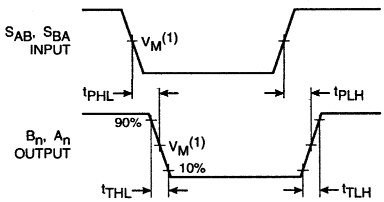


Fig.8 Waveforms showing the input S_{AB}, S_{BA} to output B_n, A_n propagation delay times and output transition times.

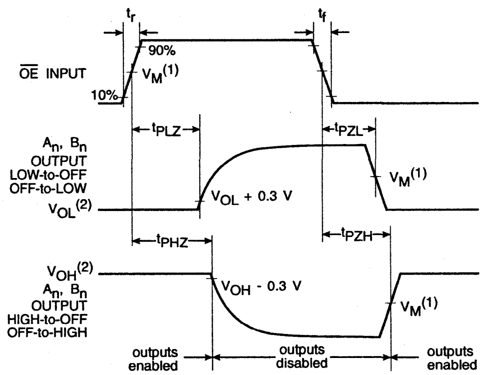


Fig.9 Waveforms showing the input $\overline{OE}$ to output A_n, B_n 3-state enable and disable times.

Notes:

(1) $V_M = 0.6$ V at $V_{CC} = 1.2$ V.
$V_M = 1.0$ V at $V_{CC} = 2.0$ V.
$V_M = 1.5$ V at $V_{CC} = 3.0$ V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

AC WAVEFORMS *(Continued)*

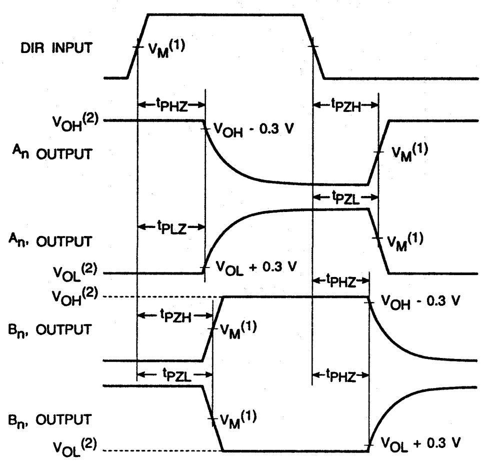


Fig.10 Waveforms showing the input DIR to output A_n, B_n 3-state enable and disable times.

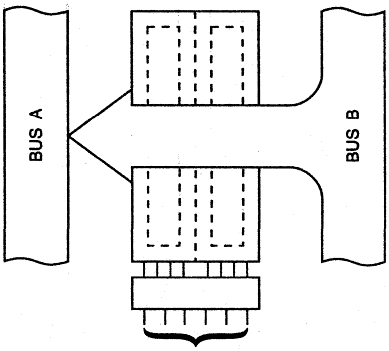
Notes:

(1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

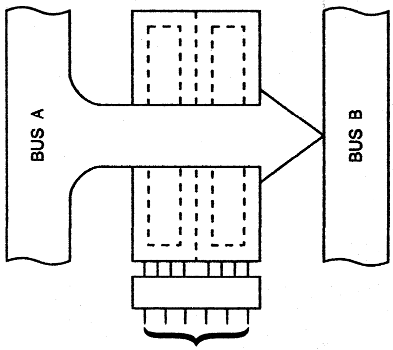
APPLICATION INFORMATION

Real-time transfer; bus B to bus A



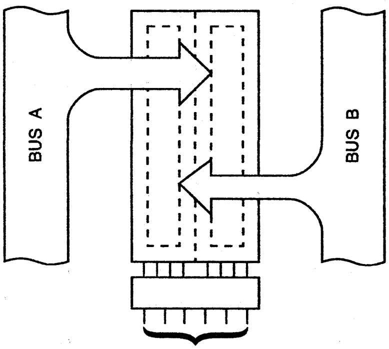
(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
L	L	X	X	X	L

Real-time transfer; bus A to bus B



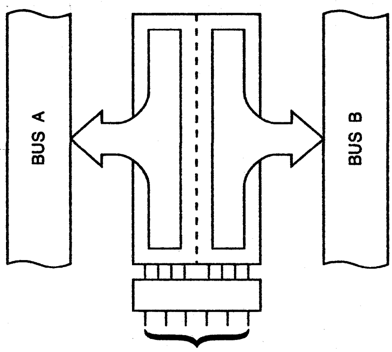
(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
L	H	X	X	L	X

Storage from A, B or A and B



(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

Transfer storage data to A or B



(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
L	L	X	H or L	X	H
L	H	H or L	X	H	X

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**

DESCRIPTION

The 74HL33648 consist of 8 inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the 'A' or 'B' bus will be clocked in the internal registers, as the appropiate clock (CP_{AB} or CP_{BA}) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the 'A' or 'B' register, or in both.The select source inputs (S_{AB} and S_{BA}) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when $\overline{OE}$ is active (LOW). In the isolation mode ($\overline{OE}$ = HIGH), '$\overline{A}$' data may be stored in the 'B' register and/or '$\overline{B}$' data may be stored in the 'A' register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, 'A' or 'B' may be driven at a time.

The '648' is functionally identical to the '646', but has inverting data paths.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	C_L = 50 pF V_{CC} = 3.3 V	3.4	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33648D	28	SO	plastic	SO28/SOT136A
74HL33648DB	28	SSOP	plastic	SSOP28/SOT341

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 3, 4, 5, 10, 11, 12, 13	$\overline{A}_0$ to $\overline{A}_7$	'$\overline{A}$' data inputs/outputs
6, 7, 8, 9	GND	ground (0 V)
14	DIR	direction control input
15	S_{BA}	select 'B' to 'A' source input
16	CP_{BA}	'B' to 'A' clock input (Low-to-High, edge-triggered)
26, 25, 24, 23, 20, 19, 18, 17	$\overline{B}_0$ to $\overline{B}_7$	'$\overline{B}$' data inputs/outputs
21, 22	V_{CC}	positive supply voltage
27	S_{AB}	select 'A' to 'B' source input
28	CP_{AB}	'A' to 'B' clock input (Low-to-High, edge-triggered)

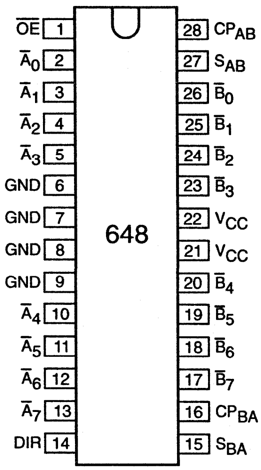


Fig.1 Pin configuration.

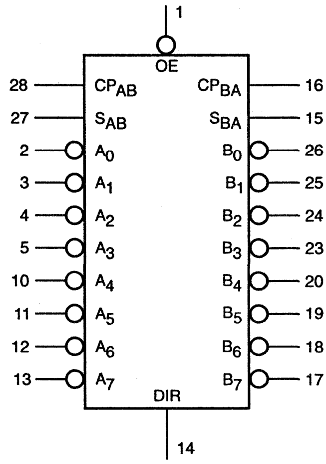


Fig.2 Logic symbol.

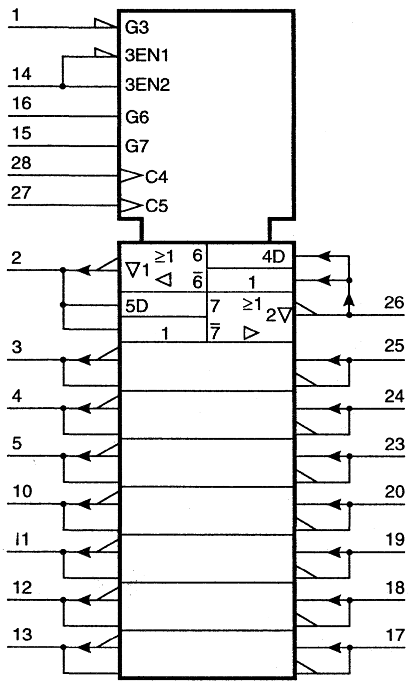


Fig.3 IEC logic symbol.

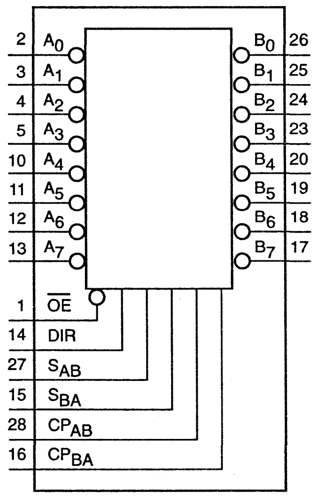


Fig.4 Functional diagram.

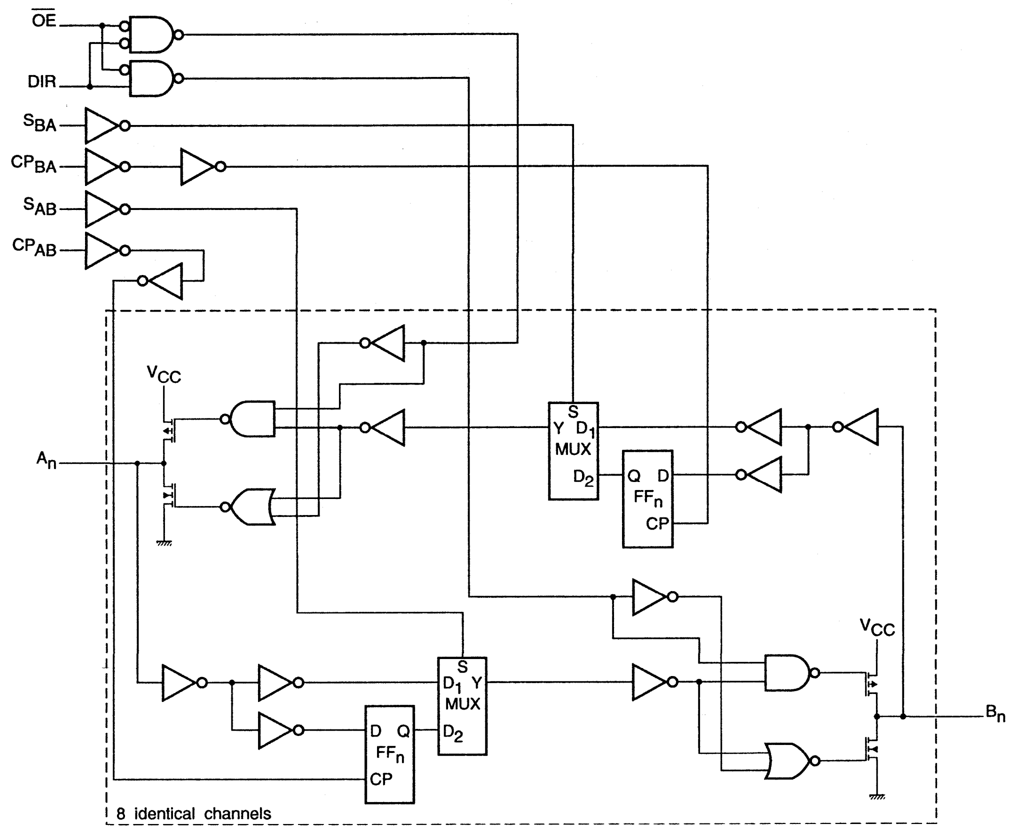


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	$\overline{A}_0$ to $\overline{A}_7$	$\overline{B}_0$ to $\overline{B}_7$	
X	X	↑	X	X	X	input	un*	store A, B unspecified*
X	X	X	↑	X	X	un*	input	store B, A unspecified*
H	X	↑	↑	X	X	input	input	store A and B data, isolation
H	X	H or L	H or L	X	X			hold storage
L	L	X	X	X	L	output	input	real-time $\overline{B}$ data to A bus
L	L	X	H or L	X	H			stored $\overline{B}$ data to A bus
L	H	X	X	L	X	input	output	real-time $\overline{A}$ data to B bus
L	H	H or L	X	H	X			stored $\overline{A}$ data to B bus

* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

DC characteristics for 74HL33648

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".

I_{CC} category: MSI

AC characteristics for 74HL33648

GND = 0 V; $t_r = t_f = 2.0$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)				UNIT	TEST CONDITIONS	
		+25		−40 to +85			V_{CC} (V)	WAVEFORMS
		MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$, $\overline{B}_n$ to $\overline{B}_n$, $\overline{A}_n$	– – –	19.5 7.3 4.9	– – –	22.4 8.4 5.6	ns	1.2 2.0 3.0	Fig.6
t_{PHL}/t_{PLH}	propagation delay CP_{AB}, CP_{BA} to $\overline{B}_n$, $\overline{A}_n$	– – –	22.8 8.6 5.7	– – –	26.4 9.9 6.6	ns	1.2 2.0 3.0	Fig.7
t_{PHL}/t_{PLH}	propagation delay S_{AB}, S_{BA} to $\overline{B}_n$, $\overline{A}_n$	– – –	23.2 8.7 5.8	– – –	26.8 10.1 6.7	ns	1.2 2.0 3.0	Fig.8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to $\overline{A}_n$, $\overline{B}_n$	– – –	17.8 7.5 5.4	– – –	20.7 8.5 6.5	ns	1.2 2.0 3.0	Fig.9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to $\overline{A}_n$, $\overline{B}_n$	– – –	15.0 6.4 4.7	– – –	16.7 7.0 5.1	ns	1.2 2.0 3.0	Fig.9
t_{PZH}/t_{PZL}	3-state output enable time DIR to $\overline{A}_n$, $\overline{B}_n$	– – –	21.4 8.8 6.3	– – –	23.5 9.6 6.8	ns	1.2 2.0 3.0	Fig.10
t_{PHZ}/t_{PLZ}	3-state output disable time DIR to $\overline{A}_n$, $\overline{B}_n$	– – –	17.4 7.3 5.3	– – –	19.0 7.9 5.7	ns	1.2 2.0 3.0	Fig.10
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	3.0 2.0	– –	3.7 2.5	– –	ns	2.0 3.0	Figs 6 and 8
t_{su}	set-up time $\overline{A}_n$, $\overline{B}_n$ to CP_{AB}, CP_{BA}	 0.9	– – –	 0.9	– – –	ns	1.2 2.0 3.0	Fig.7
t_h	hold time $\overline{A}_n$, $\overline{B}_n$ to CP_{AB}, CP_{BA}	 0.9	– – –	 0.9	– – –	ns	1.2 2.0 3.0	Fig.7
f_{max}	maximum clock pulse frequency	166 250	– –	135 200	– –	ns	2.0 3.0	Fig.7

AC WAVEFORMS

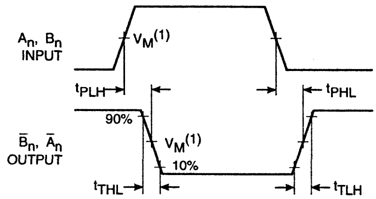


Fig.6 Waveforms showing the input A_n, B_n to output $\overline{B}_n$, $\overline{A}_n$ propagation delays and the output transition times.

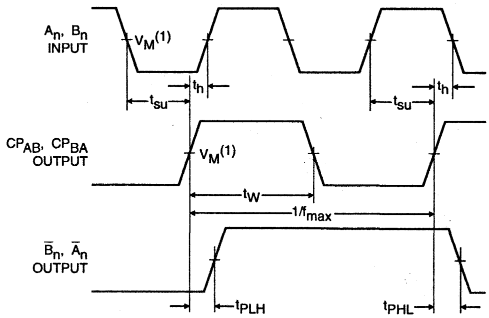


Fig.7 Waveforms showing the A_n, B_n to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output $\overline{B}_n$, $\overline{A}_n$ propagation delays.

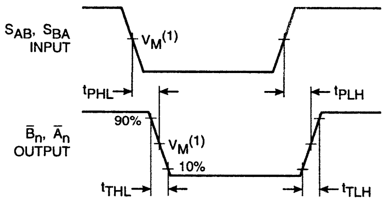


Fig.8 Waveforms showing the input S_{AB}, S_{BA} to output $\overline{B}_n$, $\overline{A}_n$ propagation delay times and output transition times.

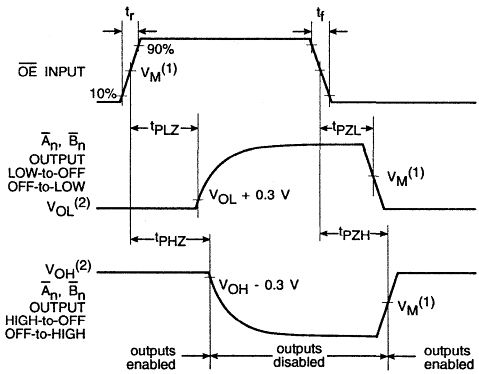


Fig.9 Waveforms showing the input $\overline{OE}$ to output $\overline{A}_n$, $\overline{B}_n$ 3-state enable and disable times.

Notes: (1) $V_M = 0.6$ V at $V_{CC} = 1.2$ V.
$V_M = 1.0$ V at $V_{CC} = 2.0$ V.
$V_M = 1.5$ V at $V_{CC} = 3.0$ V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

AC WAVEFORMS *(Continued)*

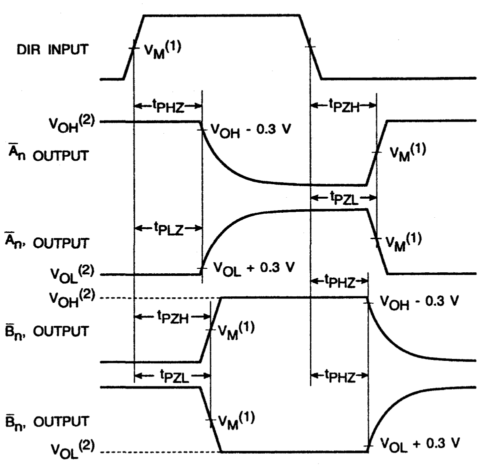


Fig.10 Waveforms showing the input DIR to output A_n, B_n 3-state enable and disable times.

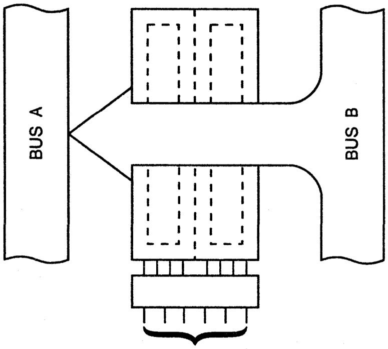
Notes:

(1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

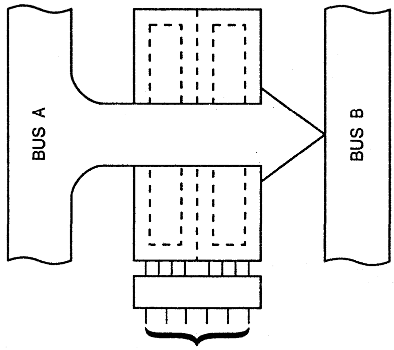
APPLICATION INFORMATION

Real-time transfer; bus B to bus A



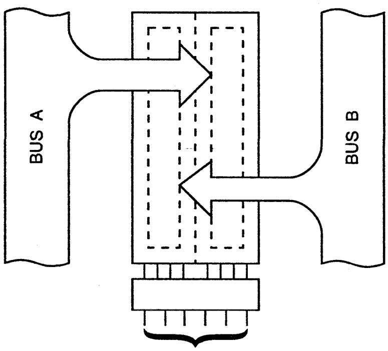
(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
L	L	X	X	X	L

Real-time transfer; bus A to bus B



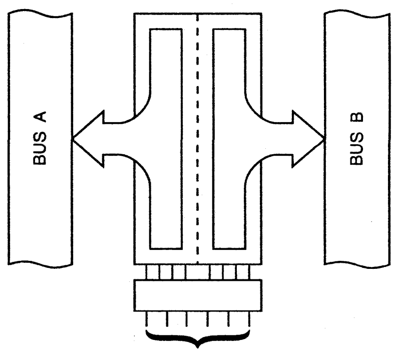
(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
L	H	X	X	L	X

Storage from A, B or A and B



(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
X	X	$\uparrow$	X	X	X
X	X	X	$\uparrow$	X	X
H	X	$\uparrow$	$\uparrow$	X	X

Transfer storage data to A or B



(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
L	L	X	H or L	X	H
L	H	H or L	X	H	X

Octal transceiver/register with dual enable; 3-state; inverting

74HL33651

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**

DESCRIPTION

The 74HL33651 consist of 8 inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the "A" or "B" or both buses, will be stored in the internal registers, at the appropiate clock inputs (CP_{AB} or CP_{BA}) regardless of the select inputs (S_{AB} and S_{BA}) or output enable (OE_{AB} and $\overline{OE}_{BA}$) control inputs. Depending on the select inputs S_{AB} and S_{BA} data can directly go from input to output (real time mode) or data can be controlled by the clock (storage mode), this is when the OE_n inputs this operating mode permits. The output enable inputs OE_{AB} and $\overline{OE}_{BA}$ determine the operation mode of the transceiver. When OE_{AB} is LOW, no data transmission from A_n to B_n is possible and when $\overline{OE}_{BA}$ is HIGH, there is no data transmission from B_n to A_n possible. When S_{AB} and S_{BA} are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE_{AB} and $\overline{OE}_{BA}$. In this configuration each output reinforces its input.

The '651' is functionally identical to the '652', but has inverting data paths.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	C_L = 50 pF V_{CC} = 3.3 V	3.4	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33651D	28	SO	plastic	SO28/SOT136A
74HL33651DB	28	SSOP	plastic	SSOP28/SOT341

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	OE_{AB}	output enable A to B input
2, 3, 4, 5, 10, 11, 12, 13	$\overline{A}_0$ to $\overline{A}_7$	'A' data inputs/outputs
6, 7, 8, 9	GND	ground (0 V)
14	$\overline{OE}_{BA}$	output enable B to A input (active LOW)
15	S_{BA}	select 'B' to 'A' source input
16	CP_{BA}	'B' to 'A' clock input (Low-to-High, edge-triggered)
26, 25, 24, 23, 20, 19, 18, 17	$\overline{B}_0$ to $\overline{B}_7$	'B' data inputs/outputs
21, 22	V_{CC}	positive supply voltage
27	S_{AB}	select 'A' to 'B' source input
28	CP_{AB}	'A' to 'B' clock input (Low-to-High, edge-triggered)

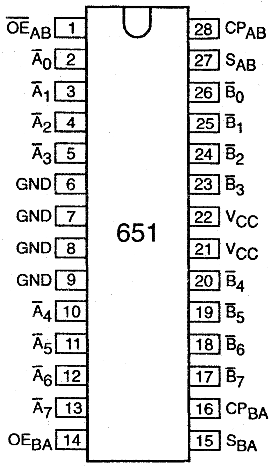


Fig.1 Pin configuration.

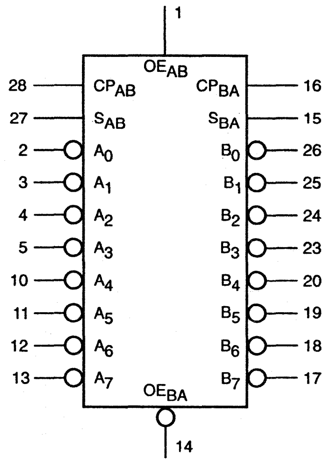


Fig.2 Logic symbol.

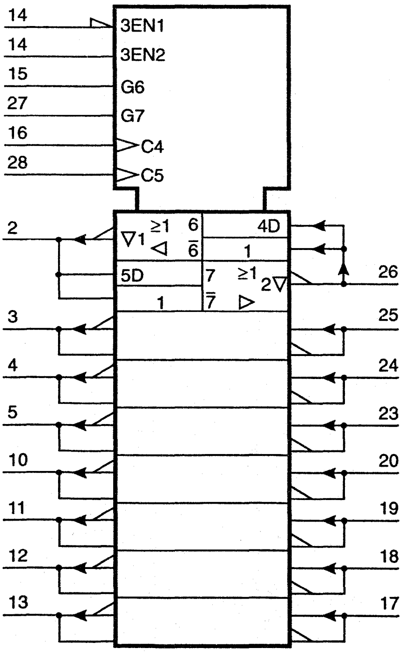


Fig3. IEC logic symbol.

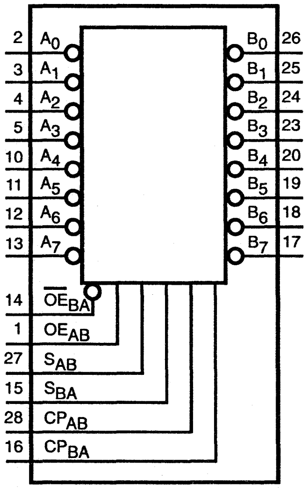


Fig.4 Functional diagram.

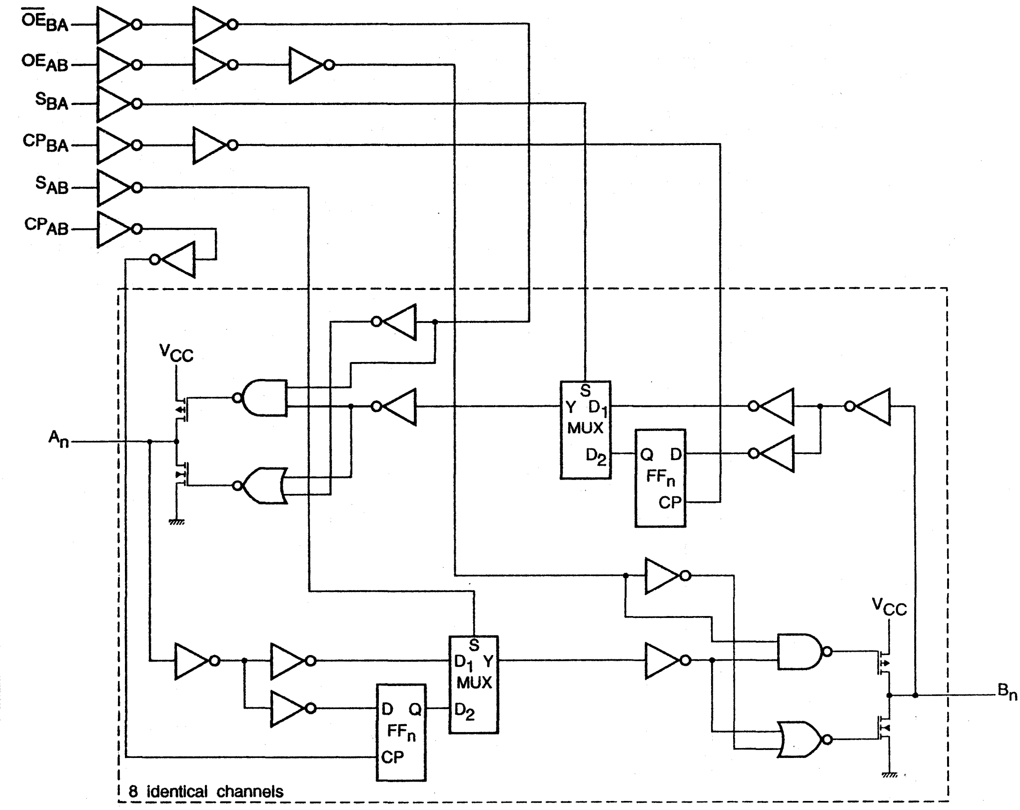


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	$\overline{A}_0$ to $\overline{A}_7$	$\overline{B}_0$ to $\overline{B}_7$	
L	H	H or L	H or L	X	X	input	input	isolation
L	H	$\uparrow$	$\uparrow$	X	X			store $\overline{A}$ and $\overline{B}$ data
X	H	$\uparrow$	H or L	X	X	input	un*	store A, hold B
H	H	$\uparrow$	$\uparrow$	L	X	input	output	store A in both registers
L	X	H or L	$\uparrow$	X	X	un*	input	hold A, store B
L	L	$\uparrow$	$\uparrow$	X	L	output	input	store B in both registers
L	L	X	X	X	L	output	input	real time $\overline{B}$ data to A bus
L	L	X	H or L	X	H			stored $\overline{B}$ data to A bus
H	H	X	X	L	X	input	output	real-time $\overline{A}$ data to B bus
H	H	H or L	X	H	X			stored $\overline{A}$ data to B bus
H	L	H or L	H or L	H	H	output	output	stored $\overline{A}$ data to B bus and stored $\overline{B}$ data to A bus

* The data output functions may be enabled or disabled by various signals at the OE_{AB} and $\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
$\uparrow$ = LOW-to-HIGH level transition

DC characteristics for 74HL33651

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".
I_{CC} category: MSI

AC characteristics for 74HL33651

GND = 0 V; $t_r = t_f = 2.0$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) +25 MIN.	T_{amb} (°C) +25 MAX.	T_{amb} (°C) -40 to +85 MIN.	T_{amb} (°C) -40 to +85 MAX.	UNIT	TEST CONDITIONS V_{CC} (V)	TEST CONDITIONS WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay $\overline{A}_n$, $\overline{B}_n$ to $\overline{B}_n$, $\overline{A}_n$	– – –	19.5 7.3 4.9	– – –	22.4 8.4 5.6	ns	1.2 2.0 3.0	Fig.6
t_{PHL}/t_{PLH}	propagation delay CP_{AB}, CP_{BA} to $\overline{B}_n$, $\overline{A}_n$	– – –	22.8 8.6 5.7	– – –	26.4 9.9 6.6	ns	1.2 2.0 3.0	Fig.7
t_{PHL}/t_{PLH}	propagation delay S_{AB}, S_{BA} to $\overline{B}_n$, $\overline{A}_n$	– – –	23.2 8.7 5.8	– – –	26.8 10.1 6.7	ns	1.2 2.0 3.0	Fig.8
t_{PZH}/t_{PZL}	3-state output enable time OE_{AB} to $\overline{B}_n$	– – –	13.1 5.7 4.2	– – –	14.3 6.1 4.5	ns	1.2 2.0 3.0	Fig.9
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{AB} to $\overline{B}_n$	– – –	14.3 6.1 4.5	– – –	15.5 6.6 4.8	ns	1.2 2.0 3.0	Fig.9
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to $\overline{A}_n$	– – –	12.3 5.4 4.0	– – –	13.5 5.8 4.3	ns	1.2 2.0 3.0	Fig.9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$ to $\overline{A}_n$	– – –	12.3 5.4 4.0	– – –	13.9 6.0 4.3	ns	1.2 2.0 3.0	Fig.9
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	2.0	– –	2.5	– –	ns	2.0 3.0	Figs 6 and 8
t_{su}	set-up time $\overline{A}_n$, $\overline{B}_n$ to CP_{AB}, CP_{BA}	0.9	– – –	0.9	– – –	ns	1.2 2.0 3.0	Fig.7
t_h	hold time $\overline{A}_n$, $\overline{B}_n$ to CP_{AB}, CP_{BA}	0.9	– – –	0.9	– – –	ns	1.2 2.0 3.0	Fig.7
f_{max}	maximum clock pulse frequency	166 250	– –	135 200	– –	MHz	2.0 3.0	Fig.7

AC WAVEFORMS

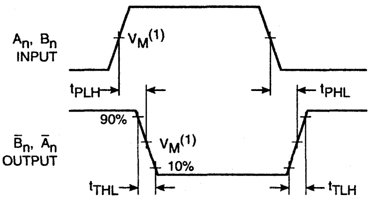


Fig.6 Waveforms showing the input A_n, B_n to output B_n, A_n propagation delays and the output transition times.

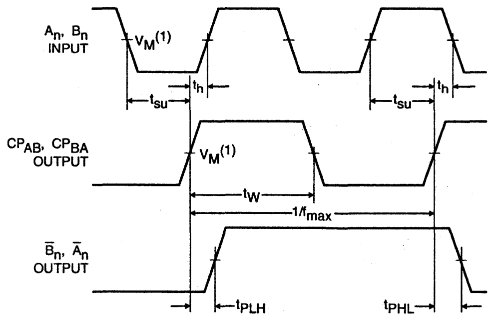


Fig.7 Waveforms showing the A_n, B_n to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output B_n, A_n propagation delays.

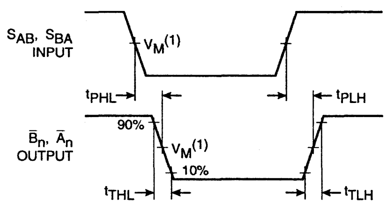


Fig.8 Waveforms showing the input S_{AB}, S_{BA} to output B_n, A_n propagation delay times and output transition times.

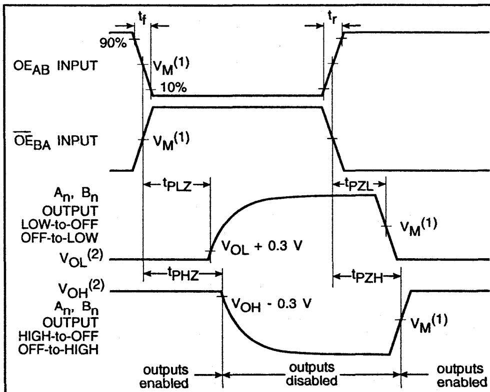


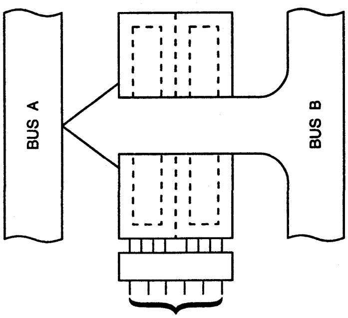
Fig.9 Waveforms showing the OE inputs (OE_{AB}, $\overline{OE}_{BA}$) to outputs A_n, B_n enable and disable times and the input rise and fall times.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

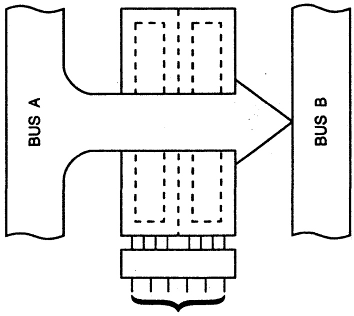
APPLICATION INFORMATION

Real-time transfer; bus B to bus A



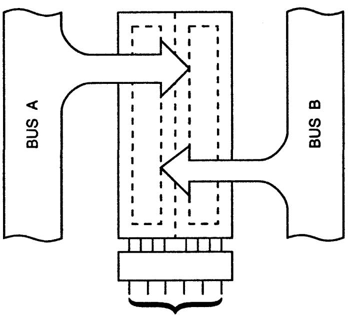
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	L	X	X	X	L

Real-time transfer; bus A to bus B



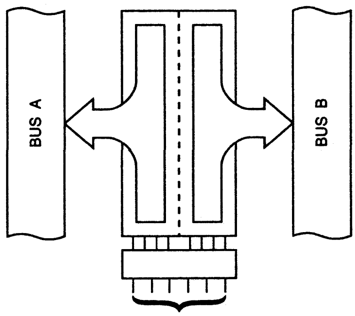
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	H	X	X	L	X

Storage from A, B or A and B



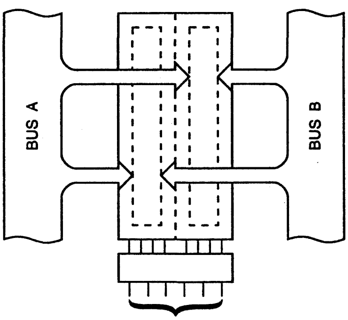
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
X	X	$\uparrow$	X	X	X
X	X	X	$\uparrow$	X	X
H	X	$\uparrow$	$\uparrow$	X	X

Transfer storage data to A or B



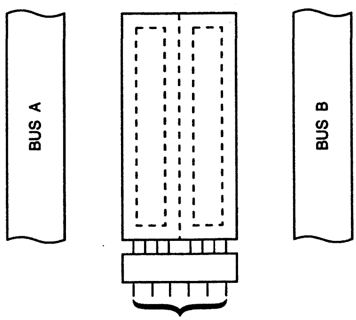
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	L	X	H or L	X	H
L	H	H or L	X	H	X

Store bus A in both registers or store bus B in both registers



OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	$\uparrow$	$\uparrow$	L	X
L	L	$\uparrow$	$\uparrow$	X	L

Isolation



OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	H	H or L	H or L	X	X

Intentionally blank

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**

DESCRIPTION

The 74HL33652 consist of 8 non-inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the "A" or "B" or both buses, will be stored in the internal registers, at the appropiate clock inputs (CP_{AB} or CP_{BA}) regardless of the select inputs (S_{AB} and S_{BA}) or output enable (OE_{AB} and $\overline{OE}_{BA}$) control inputs. Depending on the select inputs S_{AB} and S_{BA} data can directly go from input to output (real time mode) or data can be controlled by the clock (storage mode), this is when the OE_n inputs this operating mode permits. The output enable inputs OE_{AB} and $\overline{OE}_{BA}$ determine the operation mode of the transceiver. When OE_{AB} is LOW, no data transmission from A_n to B_n is possible and when $\overline{OE}_{BA}$ is HIGH, there is no data transmission from B_n to A_n possible. When S_{AB} and S_{BA} are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE_{AB} and $\overline{OE}_{BA}$. In this configuration each output reinforces its input.

The '652' is functionally identical to the '651', but has non-inverting data paths.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	C_L = 50 pF V_{CC} = 3.3 V	3.2	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74HL33652D	28	SO	plastic	SO28/SOT136A
74HL33652DB	28	SSOP	plastic	SSOP28/SOT341

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	OE_{AB}	output enable A to B input
2, 3, 4, 5, 10, 11, 12, 13	A_0 to A_7	'A' data inputs/outputs
6, 7, 8, 9	GND	ground (0 V)
14	$\overline{OE}_{BA}$	output enable B to A input (active LOW)
15	S_{BA}	select 'B' to 'A' source input
16	CP_{BA}	'B' to 'A' clock input (Low-to-High, edge-triggered)
26, 25, 24, 23, 20, 19, 18, 17	B_0 to B_7	'B' data inputs/outputs
21, 22	V_{CC}	positive supply voltage
27	S_{AB}	select 'A' to 'B' source input
28	CP_{AB}	'A' to 'B' clock input (Low-to-High, edge-triggered)

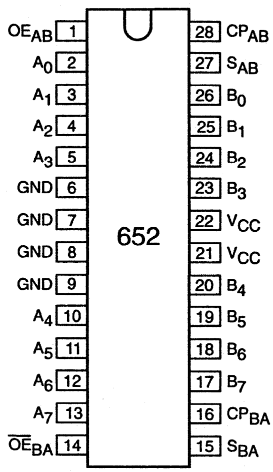


Fig.1 Pin configuration.

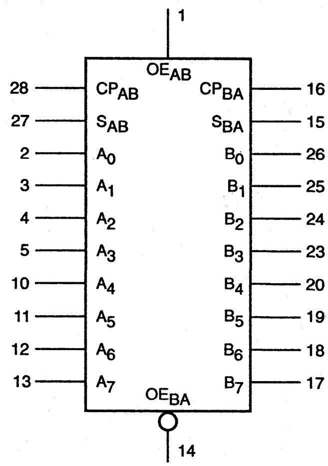


Fig.2 Logic symbol.

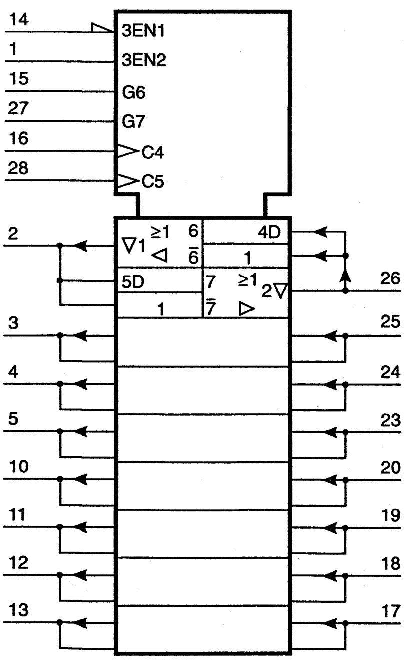


Fig3. IEC logic symbol.

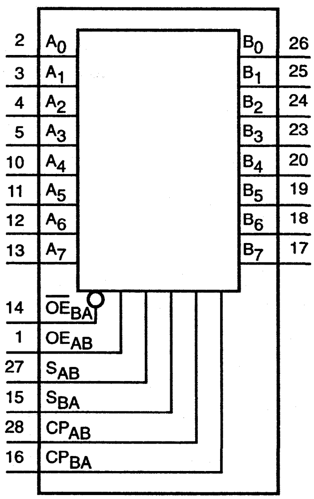


Fig.4 Functional diagram.

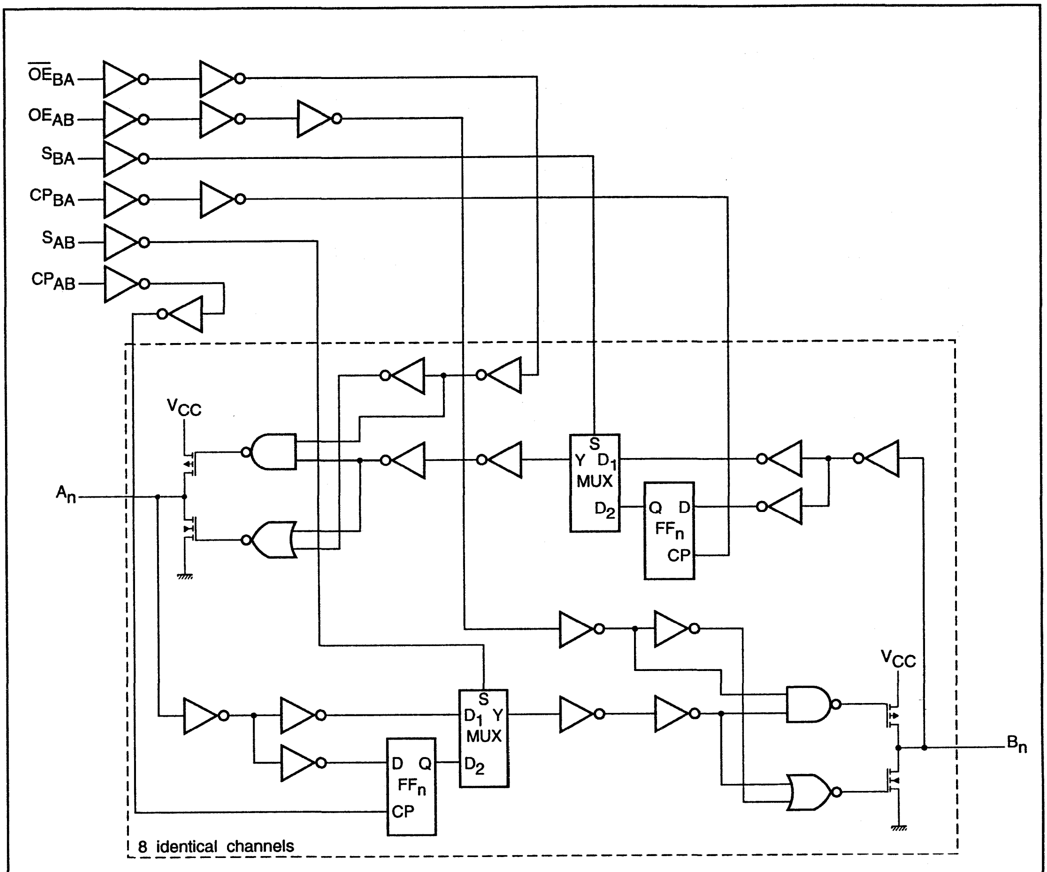


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_0 to A_7	B_0 to B_7	
L L	H H	H or L ↑	H or L ↑	X X	X X	input	input	isolation store A and B data
X H	H H	↑ ↑	H or L ↑	X L	X X	input input	un* output	store A, hold B store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X L	un* output	input input	hold A, store B store B in both registers
L L	L L	X X	X H or L	X X	L H	output	input	real time B data to A bus stored B data to A bus
H H	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus
H	L	H or L	H or L	H	H	output	output	stored A data to B bus and stored B data to A bus

* The data output functions may be enabled or disabled by various signals at the OE_{AB} and $\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

DC characteristics for 74HL33652
For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".
I_{CC} category: MSI

AC characteristics for 74HL33652
GND = 0 V; $t_r = t_f = 2.0$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) +25 MIN.	T_{amb} (°C) +25 MAX.	T_{amb} (°C) -40 to +85 MIN.	T_{amb} (°C) -40 to +85 MAX.	UNIT	TEST CONDITIONS V_{CC} (V)	TEST CONDITIONS WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	– – –	18.0 6.8 4.5	– – –	20.8 7.8 5.2	ns	1.2 2.0 3.0	Fig.6
t_{PHL}/t_{PLH}	propagation delay CP_{AB}, CP_{BA} to B_n, A_n	– – –	22.8 8.6 5.7	– – –	26.4 9.9 6.6	ns	1.2 2.0 3.0	Fig.7
t_{PHL}/t_{PLH}	propagation delay S_{AB}, S_{BA} to B_n, A_n	– – –	23.2 8.7 5.8	– – –	26.8 10.1 6.7	ns	1.2 2.0 3.0	Fig.8
t_{PZH}/t_{PZL}	3-state output enable time OE_{AB} to B_n	– – –	13.1 5.7 4.2	– – –	14.3 6.1 4.5	ns	1.2 2.0 3.0	Fig.9
t_{PHZ}/t_{PLZ}	3-state output disable time OE_{AB} to B_n	– – –	14.3 6.1 4.5	– – –	15.5 6.6 4.8	ns	1.2 2.0 3.0	Fig.9
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}_{BA}$ to A_n	– – –	12.3 5.4 4.0	– – –	13.5 5.8 4.3	ns	1.2 2.0 3.0	Fig.9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}_{BA}$ to A_n	– – –	12.3 5.4 4.0	– – –	13.9 6.0 4.3	ns	1.2 2.0 3.0	Fig.9
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	2.0	– –	2.5	– –	ns	2.0 3.0	Figs 6 and 8
t_{su}	set-up time A_n, B_n to CP_{AB}, CP_{BA}	0.9	– – –	0.9	– – –	ns	1.2 2.0 3.0	Fig.7
t_h	hold time A_n, B_n to CP_{AB}, CP_{BA}	0.9	– – –	0.9	– – –	ns	1.2 2.0 3.0	Fig.7
f_{max}	maximum clock pulse frequency	166 250	– –	135 200	– –	MHz	2.0 3.0	Fig.7

AC WAVEFORMS

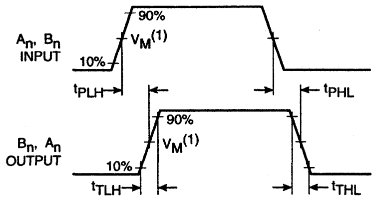


Fig.6 Waveforms showing the input A_n, B_n to output B_n, A_n propagation delays and the output transition times.

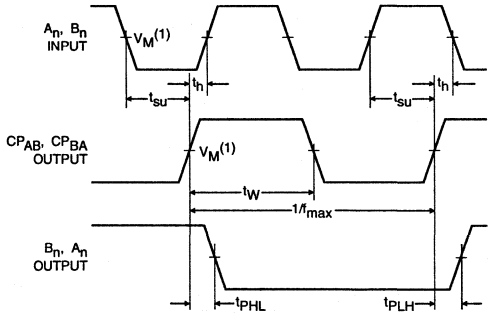


Fig.7 Waveforms showing the A_n, B_n to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output B_n, A_n propagation delays.

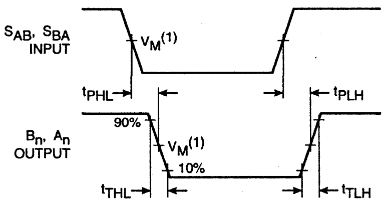


Fig.8 Waveforms showing the input S_{AB}, S_{BA} to output B_n, A_n propagation delay times and output transition times.

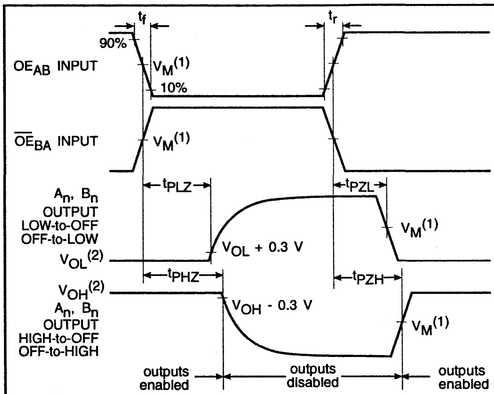


Fig.9 Waveforms showing the OE inputs (OE_{AB}, $\overline{OE}_{BA}$) to outputs A_n, B_n enable and disable times and the input rise and fall times.

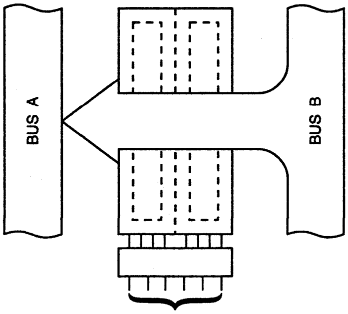
Notes:

(1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

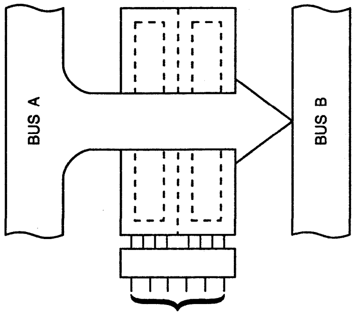
APPLICATION INFORMATION

Real-time transfer; bus B to bus A



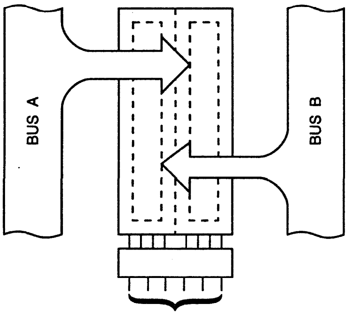
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	L	X	X	X	L

Real-time transfer; bus A to bus B



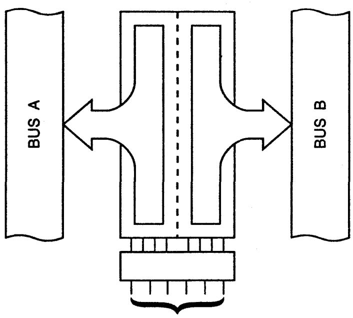
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	H	X	X	L	X

Storage from A, B or A and B



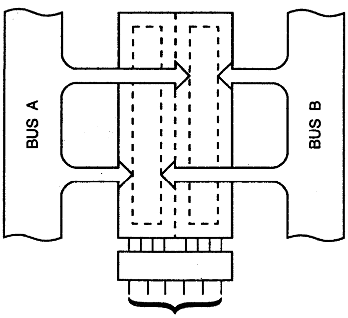
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
X	X	$\uparrow$	X	X	X
X	X	X	$\uparrow$	X	X
H	X	$\uparrow$	$\uparrow$	X	X

Transfer storage data to A or B



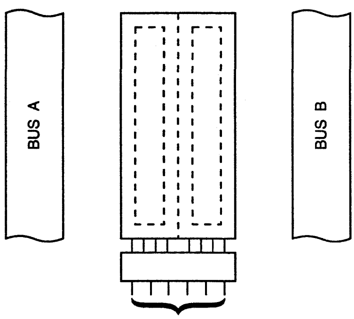
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	L	X	H or L	X	H
L	H	H or L	X	H	X

Store bus A in both registers or store bus B in both registers



OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	$\uparrow$	$\uparrow$	L	X
L	L	$\uparrow$	$\uparrow$	X	L

Isolation



OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	H	H or L	H or L	X	X

DEVICE DATA

LV-HCMOS family

Quad 2-input NAND gate 74LV00

FEATURES

- Optimized for Low Voltage applications: 1.2 to 3.6 V
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LV00 a low-voltage Si-gate CMOS device and is pin and function compatible with 74HCT00.

The 74LV00 provides the 2-input NAND function.

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF V_{CC} = 3.3 V	7	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	22	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV00N	14	DIL	plastic	DIL14/SOT27
74LV00D	14	SO	plastic	SO14/SOT108A

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

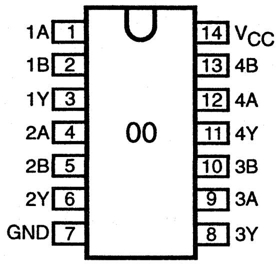


Fig.1 Pin configuration.

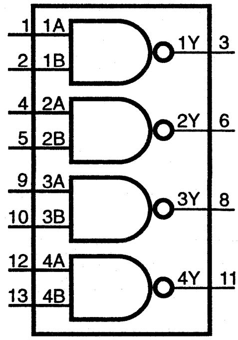


Fig.2 Logic symbol.

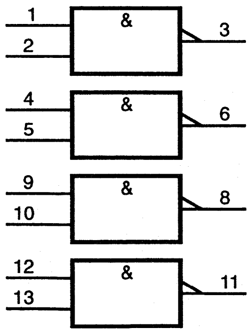


Fig.3 IEC Logic symbol.

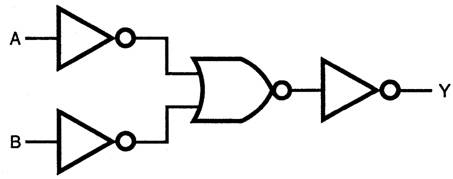


Fig.4 Logic diagram (one gate).

DC characteristics for 74LV00

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC characteristics for 74LV00

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			-40 to +85		-40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	- - -	45 15 9	- 23 14	- - -	- 28 18	- - -	- 34 21	ns	1.2 2.0 3.0	Fig. 5
t_{THL}/t_{TLH}	output transition time	- - -	25 8 5	- 16 10	- - -	- 20 13	- - -	- 24 15	ns	1.2 2.0 3.0	Fig. 5

AC WAVEFORMS

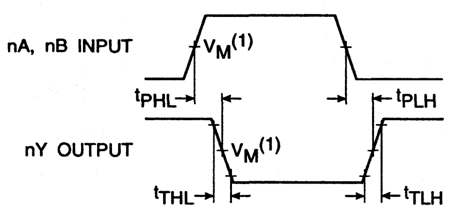


Fig. 5 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to the AC waveforms

(1) $V_M = 50\%$; V_I = GND to V_{CC}.

FEATURES

- **Optimized for Low Voltage applications: 1.2 to 3.6 V**
- **Output capability: standard**
- **I_{CC} category: SSI**

DESCRIPTION

The 74LV02 a low-voltage Si-gate CMOS device and is pin and function compatible with 74HCT02.

The 74LV02 provides the 2-input NOR function.

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF V_{CC} = 3.3 V	7	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	22	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV02N	14	DIL	plastic	DIL14/SOT27
74LV02D	14	SO	plastic	SO14/SOT108A

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1Y to 4Y	data outputs
2, 5, 8, 11	1A to 4A	data inputs
3, 6, 9, 12	1B to 4B	data inputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

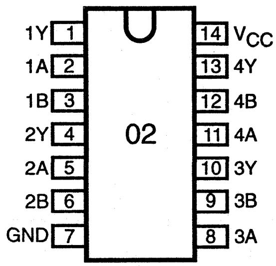


Fig.1 Pin configuration.

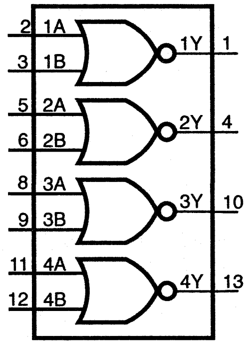


Fig.2 Logic symbol.

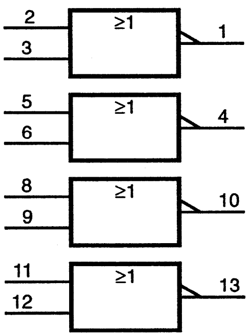


Fig.3 IEC Logic symbol.

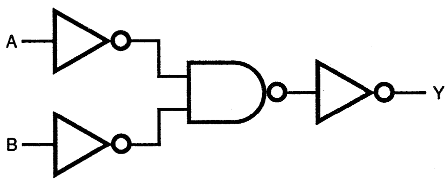


Fig.4 Logic diagram (one gate).

DC characteristics for 74LV02

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC characteristics for 74LV02

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			-40 to +85		-40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	- - -	45 15 9	- 23 14	- - -	- 28 18	- - -	- 34 21	ns	1.2 2.0 3.0	Fig. 5
t_{THL}/t_{TLH}	output transition time	- - -	25 8 5	- 16 10	- - -	- 20 13	- - -	- 24 15	ns	1.2 2.0 3.0	Fig. 5

AC WAVEFORMS

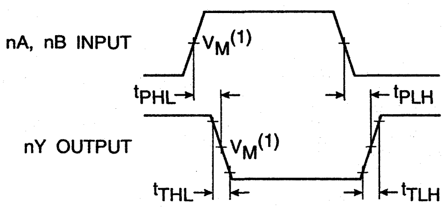


Fig. 5 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to the AC waveforms

(1) V_M = 50%; V_I = GND to V_{CC}.

FEATURES

- **Optimized for Low Voltage applications: 1.2 to 3.6 V**
- **Output capability: standard**
- **I_{CC} category: SSI**

DESCRIPTION

The 74LV04 is a low-voltage Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL).

The 74LV04 provides six inverting buffers.

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF V_{CC} = 3.3 V	7	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	21	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV04N	14	DIL	plastic	DIL14/SOT27
74LV04D	14	SO	plastic	SO14/SOT108A

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

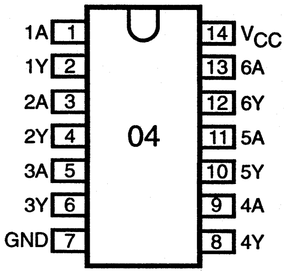


Fig.1 Pin configuration.

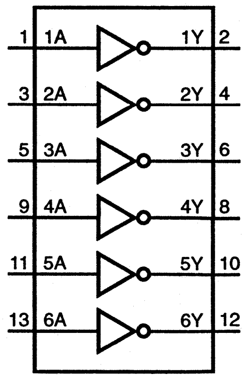


Fig.2 Logic symbol.

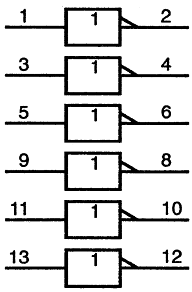


Fig.3 IEC Logic symbol.

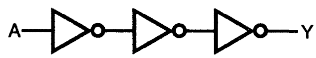


Fig.4 Logic diagram (one inverter).

DC characteristics for 74LV04

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC characteristics for 74LV04

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			-40 to +85		-40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	Propagation delay nA to nY	-	45	-	-	-	-	-	ns	1.2	Fig. 5
		-	15	23	-	28	-	34		2.0	
		-	9	14	-	18	-	21		3.0	
t_{THL}/t_{TLH}	output transition time	-	25	-	-	-	-	-	ns	1.2	Fig. 5
		-	8	16	-	20	-	24		2.0	
		-	5	10	-	13	-	15		3.0	

AC WAVEFORMS

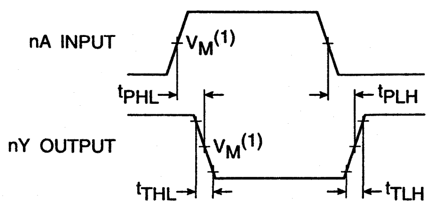


Fig. 5 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

Note to the AC waveforms

(1) V_M = 50%; V_I = GND to V_{CC}.

FEATURES

- **Optimized for Low Voltage applications: 1.2 to 3.6 V**
- **Output capability: standard**
- **I_{CC} category: SSI**

DESCRIPTION

The 74LVU04 is a low-voltage Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL).

The 74LV04 is a general purpose hex inverter. Each of the six inverters is a single stage.

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L H	H L

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF V_{CC} = 3.3 V	5	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	21	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV04N	14	DIL	plastic	DIL14/SOT27
74LV04D	14	SO	plastic	SO14/SOT108A

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

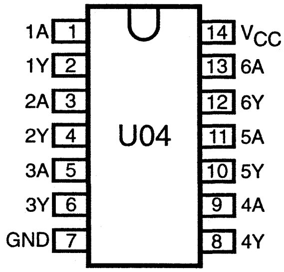


Fig.1 Pin configuration.

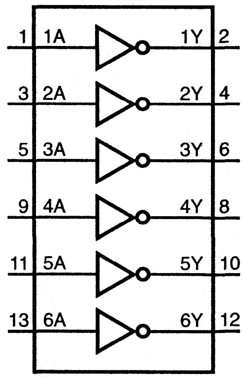


Fig.2 Logic symbol.

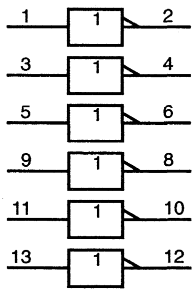


Fig.3 IEC Logic symbol.

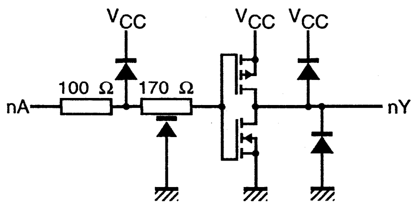


Fig.4 Logic diagram (one inverter).

DC CHARACTERISTICS FOR THE LVU04
Over recommended operating conditions
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		+25			-40 to +85		-40 to +125			V_{CC} (V)	V_I	OTHER
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.				
V_{IH}	HIGH level input voltage	1.0 1.6 2.4	- - -	- - -	1.0 1.6 2.4	- - -	1.0 1.6 2.4	- - -	V	1.2 2.0 3.0		
V_{IL}	LOW level input voltage	- - -	- - -	0.2 0.4 0.6	- - -	0.2 0.4 0.6	- - -	0.2 0.4 0.6	V	1.2 2.0 3.0		
V_{OH}	HIGH level output voltage	1.0 1.6 2.5	1.2 2.0 3.0	- - -	1.0 1.6 2.5	- - -	1.0 1.6 2.5	- - -	V	1.2 2.0 3.0	V_{IH} or V_{IL}	$-I_O$ = 20 µA
V_{OH}	HIGH level output voltage	2.48	2.82	-	2.34	-	2.20	-	V	3.0	V_{IH} or V_{IL}	$-I_O$ = 6 mA
V_{OL}	LOW level output voltage	- - -	0 0 0	0.2 0.4 0.5	- - -	0.2 0.4 0.5	- - -	0.2 0.4 0.5	V	1.2 2.0 3.0	V_{IH} or V_{IL}	I_O = 20 µA
V_{OL}	LOW level output voltage	-	0.25	0.33	-	0.4	-	0.5	V	3.0	V_{IH} or V_{IL}	I_O = 6 mA
$\pm I_I$	input leakage current	-	-	0.1	-	1.0	-	1.0	µA	3.6	V_{CC} or GND	
I_{CC}	quiescent supply current	-	-	2.0	-	20.0	-	40.0	µA	3.6	V_{CC} or GND	I_O = 0

AC characteristics for 74LV04

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			-40 to +85		-40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	Propagation delay nA to nY	-	45	-	-	-	-	-	ns	1.2	Fig. 5
		-	15	23	-	28	-	34		2.0	
		-	9	14	-	18	-	21		3.0	
t_{THL}/t_{TLH}	output transition time	-	25	-	-	-	-	-	ns	1.2	Fig. 5
		-	8	16	-	20	-	24		2.0	
		-	5	10	-	13	-	15		3.0	

AC WAVEFORMS

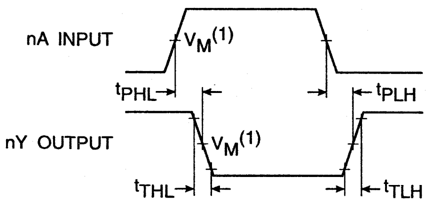


Fig. 5 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

Note to the AC waveforms

(1) V_M = 50%; V_I = GND to V_{CC}.

FEATURES

- **Optimized for Low Voltage applications: 1.2 to 3.6 V**
- **Output capability: standard**
- **I_{CC} category: SSI**

DESCRIPTION

The 74LV08 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HCT08.

The 74LV08 provides the 2-input AND function.

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF V_{CC} = 3.3 V	7	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	10	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV08N	14	DIL	plastic	DIL14/SOT27
74LV08D	14	SO	plastic	SO14/SOT108A

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

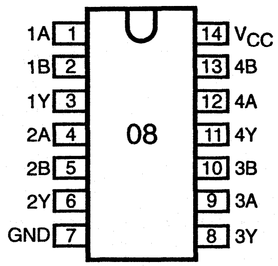


Fig.1 Pin configuration.

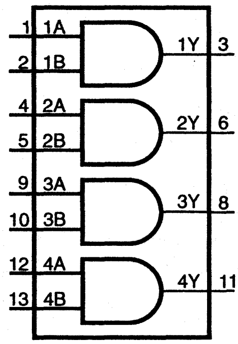


Fig.2 Logic symbol.

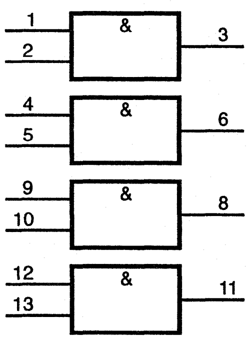


Fig.3 IEC Logic symbol.

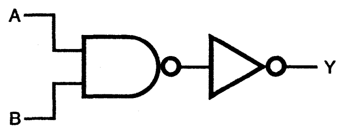


Fig.4 Logic diagram (one gate).

DC characteristics for 74LV08

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: SSI

AC characteristics for 74LV08

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	– – –	45 15 9	– 23 14	– – –	– 28 18	– – –	– 34 21	ns	1.2 2.0 3.0	Fig.5
t_{THL}/t_{TLH}	output transition time	– – –	25 8 5	- 16 10	- - -	- 20 13	- - -	- 24 15	ns	1.2 2.0 3.0	Fig.5

AC WAVEFORMS

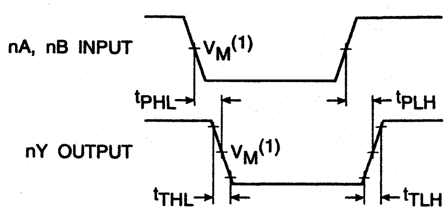


Fig.5 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to the AC waveforms

(1) V_M = 50%; V_I = GND to V_{CC}.

FEATURES

- **Optimized for Low Voltage applications: 1.2 to 3.6 V**
- **Output capability: standard**
- **I_{CC} category: SSI**

APPLICATIONS

- **Wave and pulse shapers**
- **Astable multivibrators**
- **Monostable multivibrators**

DESCRIPTION

The 74LV14 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HCT14.

The 74LV04 provides six inverting buffers with Schmitt-trigger action. They are capable of transforming slowly chaningsignals into sharply defined, jitter-free output signals.

FUNCTION TABLE

INPUT	OUTPUT
nA	**nY**
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF V_{CC} = 3.3 V	12	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	7	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV14N	14	DIL	plastic	DIL14/SOT27
74LV14D	14	SO	plastic	SO14/SOT108A

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

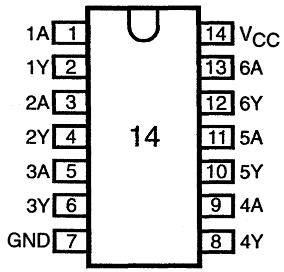


Fig.1 Pin configuration.

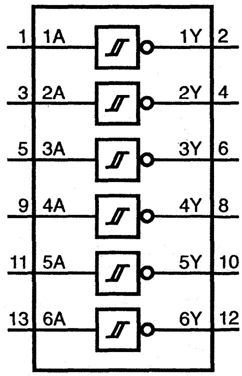


Fig.2 Logic symbol.

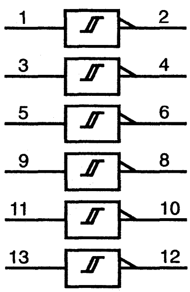


Fig.3 IEC Logic symbol.

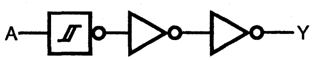


Fig.4 Logic diagram (one Schmitt-trigger).

DC characteristics for 74LV14

For the DC characteristics see chapter "LV family characteristics", section "Family specifications". Transfer characteristics are given below.
Output capability: standard
I_{CC} category: SSI

Transfer characteristics for 74LV14

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			-40 to +85		-40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
V_{T+}	positive-going threshold								V	1.2 2.0 3.0	Figs 5 and 6
V_{T-}	negative-going threshold								V	1.2 2.0 3.0	Figs 5 and 6
V_H	hysteresis ($V_{T+} - V_{T-}$)								V	1.2 2.0 3.0	Figs 5 and 6

AC characteristics for 74LV14

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			-40 to +85		-40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	Propagation delay nA to nY	- - -	60 20 12	- 30 18	- - -	- 38 23	- - -	- 45 27	ns	1.2 2.0 3.0	Fig. 7
t_{THL}/t_{TLH}	output transition time	- - -	25 8 5	- 16 10	- - -	- 20 13	- - -	- 24 15	ns	1.2 2.0 3.0	Fig. 7

TRANSFER CHARACTERISTIC WAVEFORMS

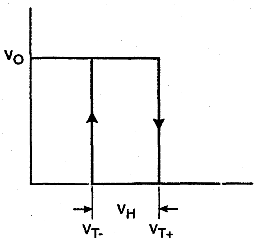


Fig.5 Transfer characteristic.

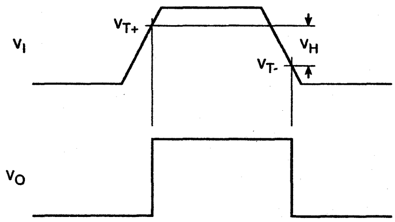


Fig. 6 Waveforms showing the definition of V_{T+}, V_{T-} and V_H; where V_{T+} and V_{T-} are between limits of 30% and 70%.

AC WAVEFORMS

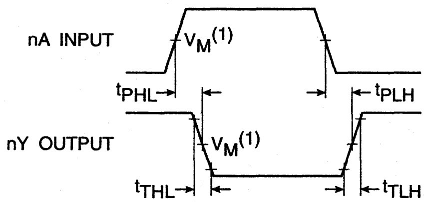


Fig. 7 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

Note to the AC waveforms

(1) V_M = 50%; V_I = GND to V_{CC}.

FEATURES

- **Optimized for Low Voltage applications: 1.2 to 3.6 V**
- **Output capability: standard**
- **I_{CC} category: SSI**

DESCRIPTION

The 74LV32 a low-voltage Si-gate CMOS device and is pin and function compatible with 74HCT32.

The 74LV32 provides the 2-input OR function.

FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF V_{CC} = 3.3 V	6	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	16	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV32N	14	DIL	plastic	DIL14/SOT27
74LV32D	14	SO	plastic	SO14/SOT108A

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

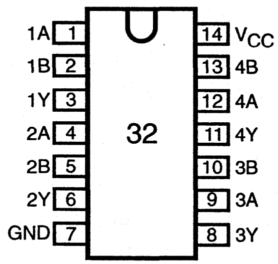


Fig.1 Pin configuration.

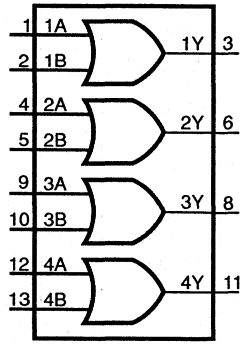


Fig.2 Logic symbol.

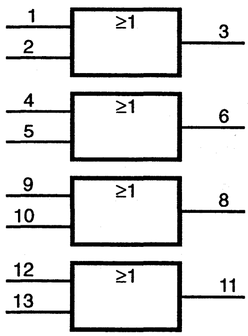


Fig.3 IEC Logic symbol.

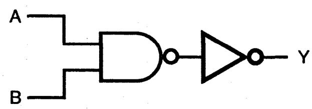


Fig.4 Logic diagram (one gate).

DC characteristics for 74LV32

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: SSI

AC characteristics for 74LV32

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			-40 to +85		-40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	Propagation delay nA, nB to nY	- - -	40 13 8	- 20 12	- - -	- 25 15	- - -	- 30 18	ns	1.2 2.0 3.0	Fig. 5
t_{THL}/t_{TLH}	output transition time	- - -	25 8 5	- 16 10	- - -	- 20 13	- - -	- 24 15	ns	1.2 2.0 3.0	Fig. 5

AC WAVEFORMS

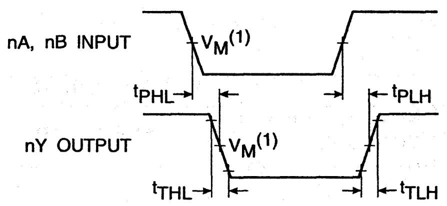


Fig. 5 Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Note to the AC waveforms

(1) V_M = 50%; V_I = GND to V_{CC}.

Dual D-type flip-flop with set and reset; positive-edge trigger

74LV74

FEATURES

- **Optimized for Low Voltage applications: 1.2 to 3.6 V**
- **Output capability: standard**
- **I_{CC} category: flip-flops**

GENERAL DESCRIPTION

The 74LV74 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HCT74.

The 74LV74 is a dual positive edge triggered, D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set ($\overline{S}_D$) and ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$ n$\overline{S}_D$ to nQ, n$\overline{Q}$ n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 15 pF V_{CC} = 3.3 V	 14 15 16	ns
f_{max}	maximum clock frequency		76	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	24	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PIN POSITION	MATERIAL	CODE
74LV74N	14	DIL	plastic	SOT27
74LV74D	14	SO	plastic	SOT108A

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	1$\overline{R}_D$, 2$\overline{R}_D$	asynchronous reset-direct input (active LOW)
2, 12	1D, 2D	data inputs
3, 11	1CP, 2CP	clock input (LOW-to-HIGH, edge-triggered)
4, 10	1$\overline{S}_D$, 2$\overline{S}_D$	asynchronous set-direct input (active LOW)
5, 9	1Q, 2Q	true flip-flop outputs
6, 8	1$\overline{Q}$, 2$\overline{Q}$	complement flip-flop outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

INPUTS				OUTPUTS	
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH CP transition
Q_{n+1} = state after the next LOW-to-HIGH CP transition

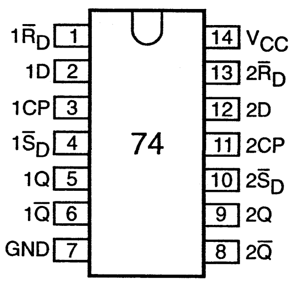


Fig.1 Pin configuration.

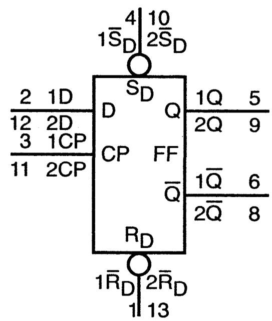


Fig.2 Logic symbol.

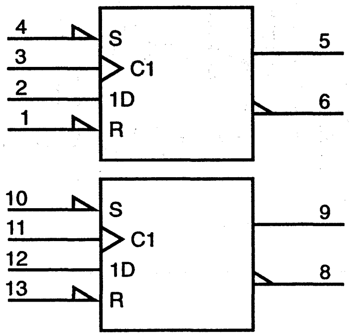


Fig.3 IEC Logic symbol.

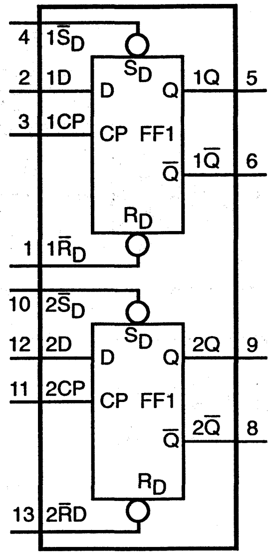


Fig.4 Logic diagram (one inverter).

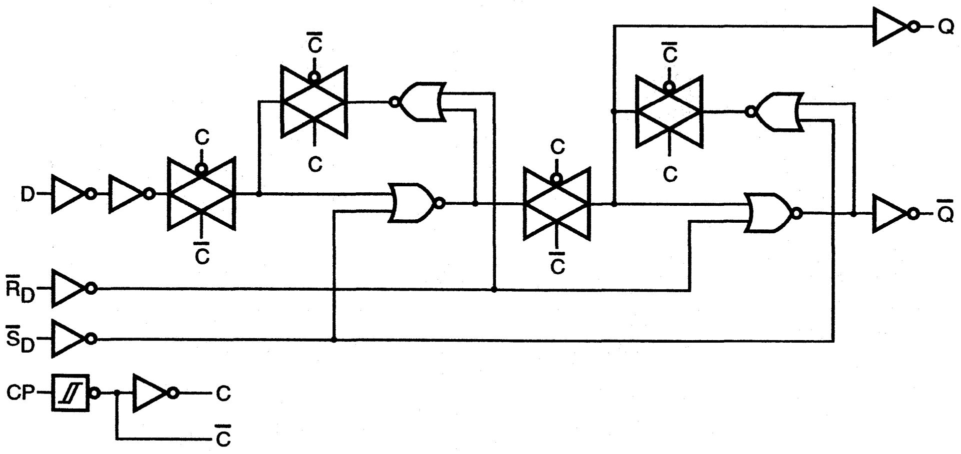


Fig.5 Logic diagram (one flip-flop).

DC characteristics for 74LV74

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC characteristics for 74LV74

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	Propagation delay nCP to nQ, n$\overline{Q}$	– – –	85 27 17	– 45 28	– – –	– 56 35	– – –	– 67 42	ns	1.2 2.0 3.0	Fig. 6
t_{PHL}/t_{PLH}	Propagation delay n$\overline{S}_D$ to nQ, n$\overline{Q}$	– – –	90 29 18	– 44 27	– – –	– 54 34	– – –	– 65 41	ns	1.2 2.0 3.0	Fig. 7
t_{PHL}/t_{PLH}	Propagation delay n$\overline{R}_D$ to nQ, n$\overline{Q}$	– – –	95 31 19	– 47 29	– – –	– 58 37	– – –	– 70 44	ns	1.2 2.0 3.0	Fig. 7
t_{THL}/t_{TLH}	Output transition time	– – –	35 10 7	– 20 15	– – –	– 25 19	– – –	– 30 23	ns	1.2 2.0 3.0	Fig. 6
t_W	clock pulse width HIGH or LOW	25 16	10 7	– –	32 20	– –	38 24	– –	ns	2.0 3.0	Fig. 6
t_W	set or reset pulse width LOW	25 16	10 7	– –	32 20	– –	38 24	– –	ns	2.0 3.0	Fig. 7
t_{rem}	removal time set or reset	– 9 6	5 2 1	– – –	– 12 8	– – –	– 15 9	– – –	ns	1.2 2.0 3.0	Fig. 7
t_{su}	set–up time nD to nCP	– 16 10	10 4 2	– – –	– 20 13	– – –	– 24 15	– – –	ns	1.2 2.0 3.0	Fig. 6
t_h	hold time nD to nCP	– 3 3	−10 −2 −2	– – –	– 3 3	– – –	– 3 3	– – –	ns	1.2 2.0 3.0	Fig. 6
f_{max}	maximum clock pulse frequency	18 30	40 70	– –	15 24	– –	12 20	– –	MHz	2.0 3.0	Fig. 6

AC WAVEFORMS

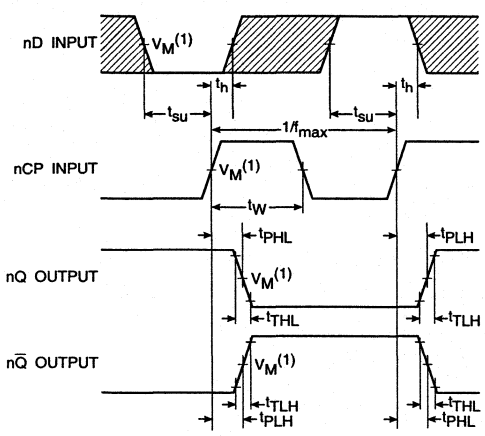


Fig. 6 Waveforms showing the clock (nCP) to output (nQ, n$\overline{Q}$) propagation delays, the clock pulse width, the nD to nCP set-up times, the nCP to nD hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig.6

The shaded areas indicate when the input is permitted to change for predictable output performance.

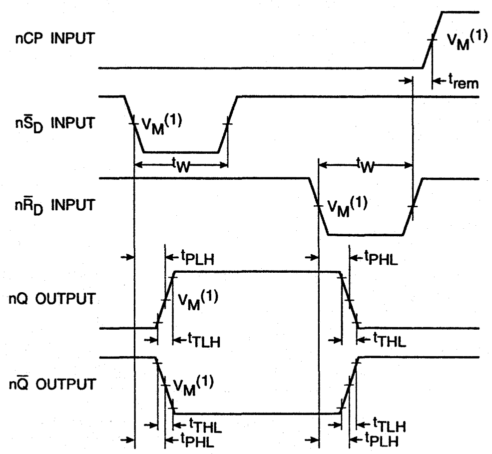


Fig.7 Waveforms showing the set (n$\overline{S}_D$) and reset (n$\overline{R}_D$) input to output (nQ, n$\overline{Q}$) propagation delays, the set and reset pulse widths and the n$\overline{R}_D$ to nCP removal time.

Note to the AC waveforms

(1) V_M = 50%; V_I = GND to V_{CC}.

FEATURES

- **Optimized for Low Voltage applications: 1.2 to 3.6 V**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV125 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HCT125.

The 74LV125 consists of four non-inverting buffers/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input ($n\overline{OE}$). A HIGH at $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA	nY
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA to nY	C_L = 15 pF V_{CC} = 3.3 V	9	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	V_{CC} = 3.3 V notes 1 and 2	22	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV125N	14	DIL	plastic	DIL14/SOT27
74LV125D	14	SO	plastic	SO14/SOT108A

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	$1\overline{OE}$ to $4\overline{OE}$	output enable inputs (active LOW)
2, 5, 9, 12	1A to 4A	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

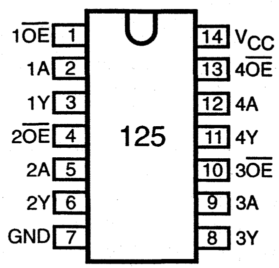


Fig.1 Pin configuration.

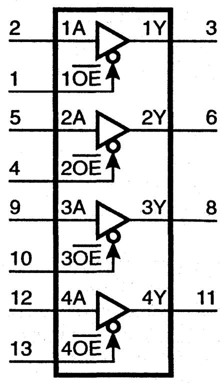


Fig.2 Logic symbol.

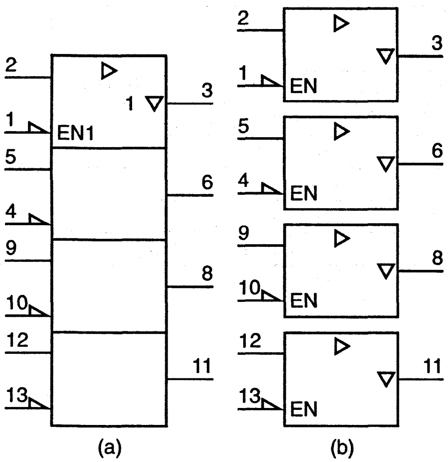


Fig.3 IEC Logic symbol.

DC characteristics for 74LV125

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC characteristics for 74LV125

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			-40 to +85		-40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	Propagation delay nA to nY	–	55	–	–	–	–	–	ns	1.2	Fig.4
		–	18	28	–	35	–	43		2.0	
		–	11	17	–	21	–	26		3.0	
t_{PZH}/t_{PZL}	3-state output enable time n$\overline{OE}$ to nY	–	75	–	–	–	–	–	ns	1.2	Fig.5
		–	25	38	–	48	–	58		2.0	
		–	15	23	–	29	–	35		3.0	
t_{PHZ}/t_{PLZ}	3-state output disable time n$\overline{OE}$ to nY	–	55	–	–	–	–	–	ns	1.2	Fig.5
		–	21	30	–	40	–	47		2.0	
		–	15	20	–	24	–	28		3.0	
t_{THL}/t_{TLH}	output transition time	–	25	-	-	-	-	-	ns	1.2	Fig.4
		–	8	16	-	20	-	24		2.0	
		–	5	10	-	13	-	15		3.0	

AC WAVEFORMS

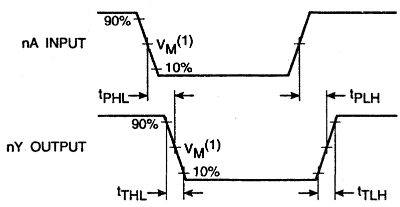


Fig.4 Waveforms showing the input (nA) to output (nY) propagation delays and the output transition times.

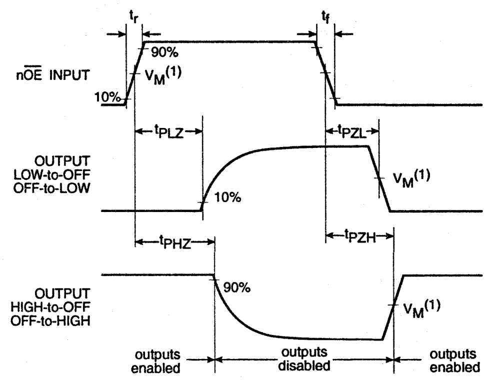


Fig.5 Waveforms showing the 3-state enable and disable times.

Note to the AC waveforms

(1) V_M = 50%; V_I = GND to V_{CC}.

FEATURES

- **Optimized for Low Voltage applications: 1.2 to 3.6 V**
- **Demultiplexing capability**
- **Multiple input enable for easy expansion**
- **Ideal for memory chip select decoding**
- **Active LOW mutually exclusive outputs**
- **Output capability: standard**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV138 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HCT138.

The 74LV138 accepts three binary weighted address inputs (A_0, A_1, A_2) and when enabled, provide 8 mutually exclusive active LOW outputs ($\overline{Y}_0$ to $\overline{Y}_7$).
The '138' features three enable inputs: two active LOW ($\overline{E}_1$ and $\overline{E}_2$ and one active HIGH (E_3). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the '138' to a 1-of-32 (5 lines to 32 lines) decoder with just four '138' ICs and one inverter. The '138' can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The '138' is identical to the '238' but has non-inverting (true) outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay An to $\overline{Y}$n, E3 to $\overline{Y}$n, $\overline{E}$n to $\overline{Y}$n	C_L = 15 pF V_{CC} = 3.3 V	12 14	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per package	V_{CC} = 3.3 V notes 1 and 2	67	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV138N	16	DIL	plastic	DIL16/SOT38Z
74LV138D	16	SO	plastic	SO16/SOT109A

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5	$\overline{E}_1$, $\overline{E}_2$	enable inputs (active LOW)
6	E_3	enable inputs (active HIGH)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y}_0$ to $\overline{Y}_7$	outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

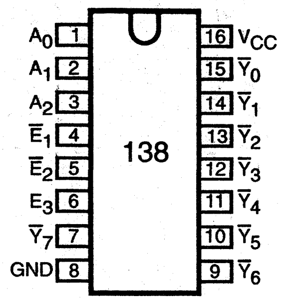


Fig.1 Pin configuration.

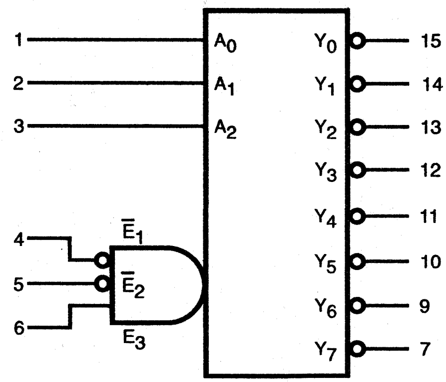


Fig.2 Logic diagram.

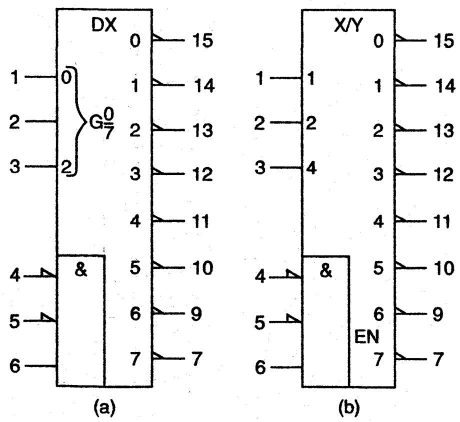


Fig.3 IEC logic symbol.

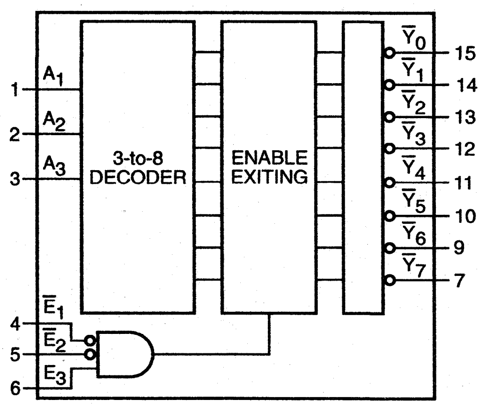


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

DC characteristics for 74LV138

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC characteristics for 74LV138

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			-40 to +85		-40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$	–	75	–	–	–	–	–	ns	1.2	Fig.5
		–	25	38	–	48	–	58		2.0	
		–	15	23	–	29	–	35		3.0	
t_{PHL}/t_{PLH}	propagation delay E_3 to $\overline{Y}_n$	–	85	–	–	–	–	–	ns	1.2	Fig.5
		–	28	43	–	55	–	65		2.0	
		–	17	26	–	33	–	39		3.0	
t_{PHL}/t_{PLH}	propagation delay $\overline{E}_n$ to $\overline{Y}_n$	–	85	–	–	–	–	–	ns	1.2	Fig.6
		–	28	43	–	55	–	65		2.0	
		–	17	26	–	33	–	39		3.0	
t_{THL}/t_{TLH}	output transition time	–	25	–	–	–	–	–	ns	1.2	Figs 5 and 6
		–	8	16	–	20	–	24		2.0	
		–	5	10	–	13	–	15		3.0	

AC WAVEFORMS

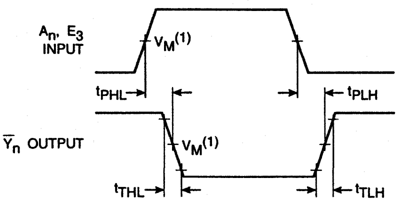


Fig. 5 Waveforms showing the address input (An) and enable input (E_3) to output ($\overline{Y}n$) propagation delays and the output transition times.

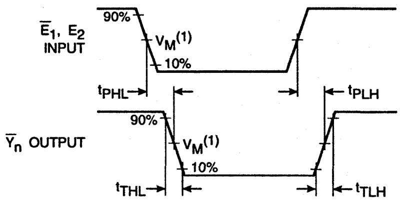


Fig. 6 Waveforms showing the enable input (E_n) to output ($\overline{Y}n$) propagation delays and the output transition times.

Note to the AC waveforms

(1) V_M = 50%; V_I = GND to V_{CC}.

FEATURES

- Optimized for Low Voltage applications: 1.2 to 3.6 V
- Demultiplexing capability
- Two independent 2-to-4 decoders
- Multifunction capability
- Active LOW mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

APPLICATIONS

- Memory decoding or data-routing
- Code conversion

DESCRIPTION

The 74LV139 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HCT139.

The 74LV139 is a dual 2-to-4 line decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (nA_0 and nA_1) and providing four mutually exclusive active LOW outputs ($n\overline{Y}_0$ to $n\overline{Y}_3$). Each decoder has an active LOW enable input ($n\overline{E}$).
When $n\overline{E}$ is HIGH, every output is forced HIGH. The enable can be used as the data input for a 1-to-4 demultiplexer application.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA_n to $n\overline{Y}_n$, $n\overline{E}$ to $n\overline{Y}_n$	C_L = 15 pF V_{CC} = 3.3 V	11 10	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	V_{CC} = 3.3 V notes 1 and 2	42	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV139N	16	DIL	plastic	DIL16/SOT38Z
74LV139D	16	SO	plastic	SO16/SOT109A

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{E}$, $2\overline{E}$	enable inputs (active LOW)
2, 3	$1A_0$, $1A_1$	address inputs
4, 5, 6, 7	$1\overline{Y}_0$ to $1\overline{Y}_3$	outputs (active LOW)
8	GND	ground (0 V)
12, 11, 10, 9	$2\overline{Y}_0$ to $2\overline{Y}_3$	outputs (active LOW)
14, 13	$2A_0$, $2A_1$	address inputs
16	V_{CC}	positive supply voltage

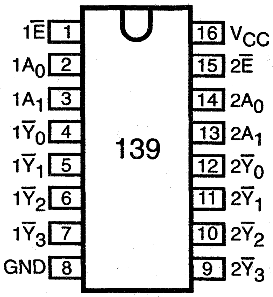


Fig.1 Pin configuration.

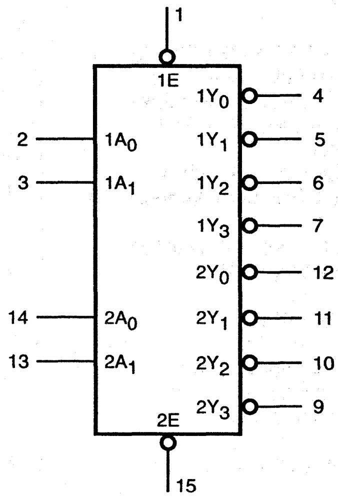


Fig.2 Logic diagram.

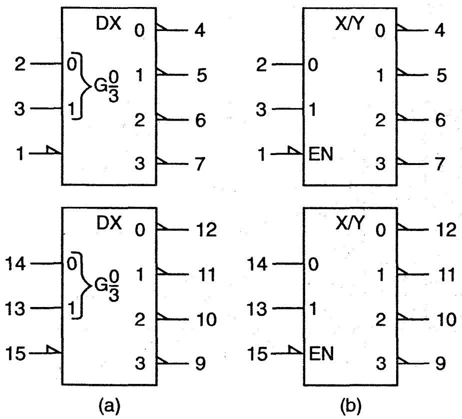


Fig.3 IEC logic symbol.

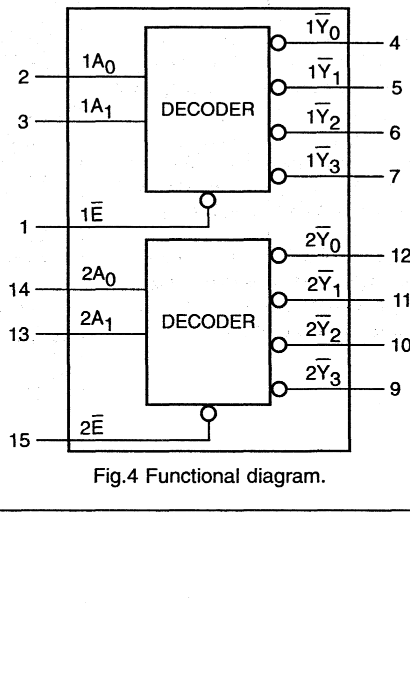


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS			OUTPUTS			
$n\overline{E}$	nA_0	nA_1	$n\overline{Y}_0$	$n\overline{Y}_1$	$n\overline{Y}_2$	$n\overline{Y}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

DC characteristics for 74LV139

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC characteristics for 74LV139

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			-40 to +85		-40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay nA_n to $\overline{Y}_n$	– – –	70 23 14	– 35 21	– – –	– 43 26	– – –	– 53 32	ns	1.2 2.0 3.0	Fig.5
t_{PHL}/t_{PLH}	propagation delay $n\overline{E}$ to $\overline{Y}_n$	– – –	60 20 12	– 30 18	– – –	– 38 23	– – –	– 45 27	ns	1.2 2.0 3.0	Fig.6
t_{THL}/t_{TLH}	output transition time	– – –	25 8 5	– 16 10	– – –	– 20 13	– – –	– 24 15	ns	1.2 2.0 3.0	Figs 5 and 6

AC WAVEFORMS

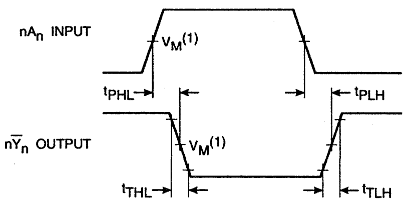


Fig. 5 Waveforms showing the address input (nA_n) to output ($n\overline{Y}n$) propagation delays and the output transition times.

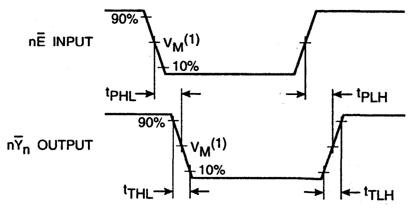


Fig. 6 Waveforms showing the enable input ($n\overline{E}$) to output ($n\overline{Y}_n$) propagation delays and the output transition times.

Note to the AC waveforms

(1) $V_M = 50\%$; V_I = GND to V_{CC}.

FEATURES

- **Optimized for Low Voltage applications: 1.2 to 3.6 V**
- **Gated serial data inputs**
- **Asynchronous master reset**
- **Output capability: standard**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV164 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HCT164.

The 74LV164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages.
Data is entered serially through one of two inputs (D_{sa} or D_{sb}); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock (CP) input and enters into Q_0, which is the logical AND of the two data inputs (D_{sa}, D_{sb}) that existed one set-up time prior to the rising clock edge.

A LOW on the master reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $\overline{CP}$ to Q_n MR to Q_n	C_L = 15 pF V_{CC} = 3.3 V	 12 11	 ns ns
f_{max}	maximum clock frequency		78	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	V_{CC} = 3.3 V notes 1 and 2	40	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV164N	14	DIL	plastic	DIL14/SOT27
74LV164D	14	SO	plastic	SO14/SOT108A

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2	D_{sa}, D_{sb}	data inputs
3, 4, 5, 6, 10, 11, 12, 13	Q_0 to Q_7	outputs
7	GND	ground (0 V)
8	CP	clock input (LOW-to-HIGH, edge-triggered)
9	$\overline{MR}$	master reset input (active LOW)
14	V_{CC}	positive supply voltage

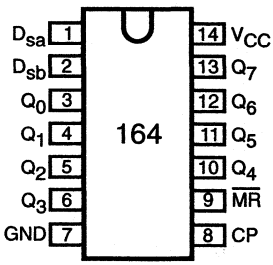


Fig.1 Pin configuration.

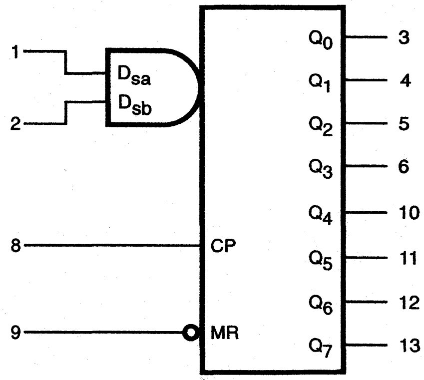


Fig.2 Logic symbol.

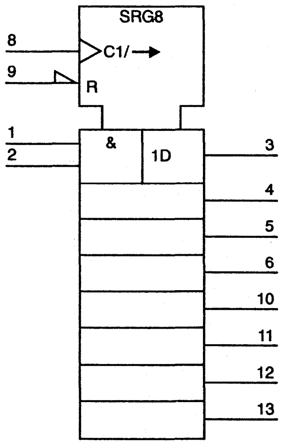


Fig.3 IEC logic symbol.

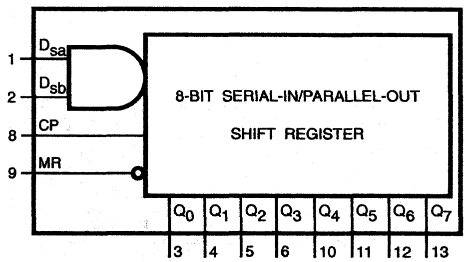


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS				OUTPUTS	
	$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	$Q_1 - Q_7$
reset (clear)	L	X	x	x	L	L – L
shift	H	↑	l	l	L	$q_0 - q_6$
	H	↑	l	h	L	$q_0 - q_6$
	H	↑	h	l	L	$q_0 - q_6$
	H	↑	h	h	H	$q_0 - q_6$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
q = lower case letters indicate the state of referenced input one set-up time prior to the LOW-to-HIGH clock transition
↑ = LOW-to-HIGH clock transition

DC characteristics for 74LV164

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC characteristics for 74LV164

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			-40 to +85		-40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	– – –	60 20 12	– 30 18	– – –	– 38 23	– – –	– 45 27	ns	1.2 2.0 3.0	Fig.5
t_{PHL}	propagation delay $\overline{MR}$ to Q_n	– – –	55 18 11	– 28 17	– – –	– 35 21	– – –	– 43 26	ns	1.2 2.0 3.0	Fig.6
t_{THL}/t_{TLH}	output transition time	– – –	25 8 5	– 16 10	– – –	– 20 13	– – –	– 24 15	ns	1.2 2.0 3.0	Fig.5
t_W	clock pulse width HIGH or LOW			– –		– –		– –	ns	2.0 3.0	Fig.5
t_W	master reset pulse width; LOW			– –		– –		– –	ns	2.0 3.0	Fig.6
t_{rem}	removal time $\overline{MR}$ to CP			– – –		– – –		– – –	ns	1.2 2.0 3.0	Fig.6
t_{su}	set-up time D_{sa}, D_{sb} to CP			– – –		– – –		– – –	ns	1.2 2.0 3.0	Fig.7
t_h	hold time D_{sa}, D_{sb} to CP			– – –		– – –		– – –	ns	1.2 2.0 3.0	Fig.7
f_{max}	maximum clock pulse frequency			– –		– –		– –	MHz	2.0 3.0	Fig.5

AC WAVEFORMS

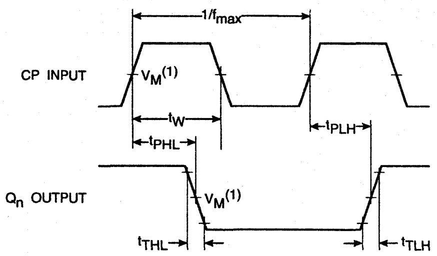


Fig.5 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

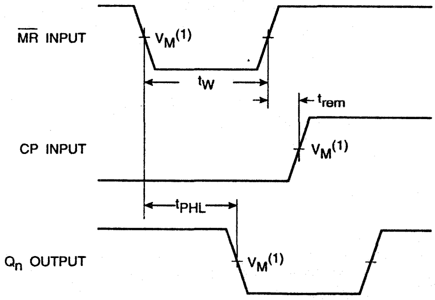


Fig.6 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to ouput (Q_n) propagation delays and the master reset to clock (CP) removal time.

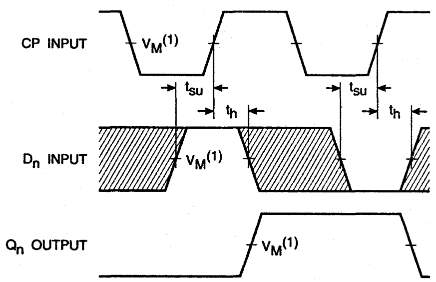


Fig.7 Waveforms showing the data set-up and hold times for D_n inputs.

Note to Fig.7
The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to the AC waveforms
(1) V_M = 50%; V_I = GND to V_{CC}.

FEATURES

- **Optimized for Low Voltage applications: 1.2 to 3.6 V**
- **Six edge-triggered D-type flip-flops**
- **Asynchronous master reset**
- **Output capability: standard**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV174 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HCT174.

The 74LV174 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one set-up time prior to the LOW-to-HIGH clock transition, is transferred to the corresponding output of the flip-flop.

A LOW level on the $\overline{MR}$ input forces all outputs LOW, independently of clock or data inputs.

The device is useful for applications requiring true outputs only and clock and master reset inputs that are common to all storage elements.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n $\overline{MR}$ to Q_n	C_L = 15 pF V_{CC} = 3.3 V	 17 13	 ns ns
f_{max}	maximum clock frequency		99	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	V_{CC} = 3.3 V notes 1 and 2	17	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV174N	14	DIL	plastic	DIL16/SOT38Z
74LV174D	14	SO	plastic	SO14/SOT109A

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	asynchronous master reset (active LOW)
2, 5, 7, 10, 12, 15	Q_0 to Q_5	flip-flop outputs
3, 4, 6, 11, 13, 14	D_0 to D_5	data inputs
8	GND	ground (0 V)
9	CP	clock input (LOW-to-HIGH, edge-triggered)
16	V_{CC}	positive supply voltage

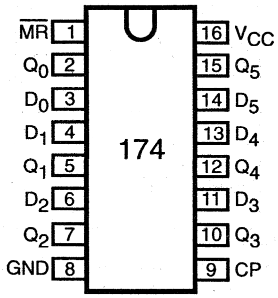


Fig.1 Pin configuration.

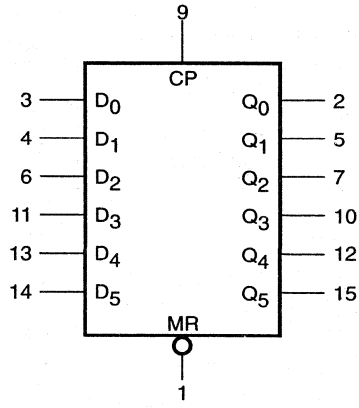


Fig.2 Logic symbol.

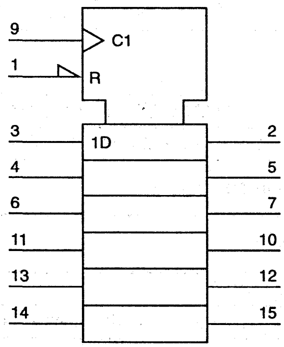


Fig.3 IEC logic symbol.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
reset (clear)	L	X	X	L
load "1"	H	↑	h	H
load "0"	H	↑	l	L

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
q = lower case letter indicate the state of referenced input one set-up time prior to the LOW-to-HIGH clock transition
↑ = LOW-to-HIGH clock transition

DC characteristics for 74LV174

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC characteristics for 74LV174

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	–	100	–	–	–	–	–	ns	1.2	Fig.5
		–	33	50	–	63	–	75		2.0	
		–	20	30	–	38	–	45		3.0	
t_{PHL}	propagation delay $\overline{MR}$ to Q_n	–	80	–	–	–	–	–	ns	1.2	Fig.6
		–	27	40	–	50	–	60		2.0	
		–	16	24	–	30	–	36		3.0	
t_{THL}/t_{TLH}	output transition time	–	25	–	–	–	–	–	ns	1.2	Fig.5
		–	8	16	–	20	–	24		2.0	
		–	5	10	–	13	–	15		3.0	
t_W	clock pulse width HIGH or LOW	–	–	–	–	–	–	–	ns	2.0	Fig.5
		16	6	–	20	–	24	–		3.0	
t_W	master reset pulse width LOW	–	–	–	–	–	–	–	ns	2.0	Fig.6
		16	4	–	20	–	24	–		3.0	
t_{rem}	removal time $\overline{MR}$ to CP	–	–	–	–	–	–	–	ns	1.2	Fig.6
		–	–	–	–	–	–	–		2.0	
		5	−4	–	5	–	5	–		3.0	
t_{su}	set–up time D_n to CP	–	–	–	–	–	–	–	ns	1.2	Fig.7
		–	–	–	–	–	–	–		2.0	
		12	2	–	15	–	18	–		3.0	
t_h	hold time D_n to CP	–	–	–	–	–	–	–	ns	1.2	Fig.7
		–	–	–	–	–	–	–		2.0	
		3	−2	–	3	–	3	–		3.0	
f_{max}	maximum clock pulse frequency	–	–	–	–	–	–	–	MHz	2.0	Fig. 5
		30	90	–	24	–	20	–		3.0	

AC WAVEFORMS

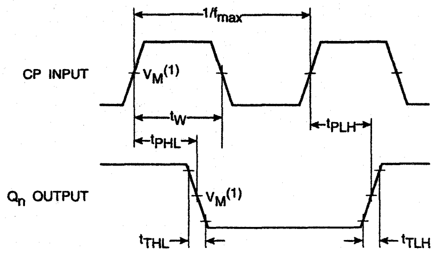


Fig.4 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

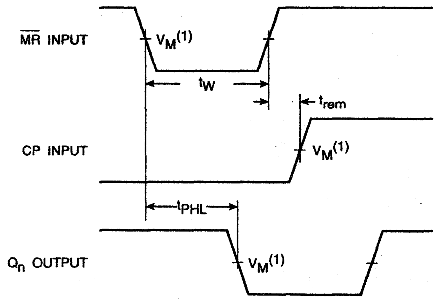


Fig.5 Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n) propagation delay and the master reset to clock removal time.

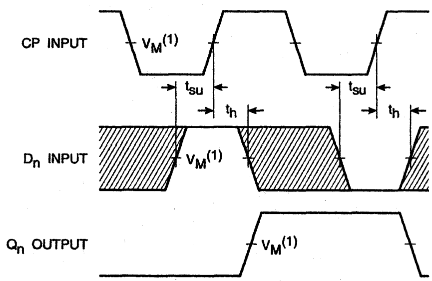


Fig.6 Waveforms showing the data set-up and hold times for the data input (D_n).

Note to Fig.6

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to the AC waveforms

(1) V_M = 50%; V_I = GND to V_{CC}.

FEATURES

- **Optimized for Low Voltage applications: 1.2 to 3.6 V**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV244 a low-voltage Si-gate CMOS device and is pin and function compatible with 74HCT244.

The 74LV244 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.
The "244" is identical to the "240" but has non-inverting outputs.

TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF V_{CC} = 3.3 V	8	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PIN POSITION	MATERIAL	CODE
74LV244N	20	DIL	plastic	SOT146
74LV244D	20	SO	plastic	SOT163A
74LV244DB	20	SSOP	plastic	SOT339

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	bus outputs
19	$2\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive power supply

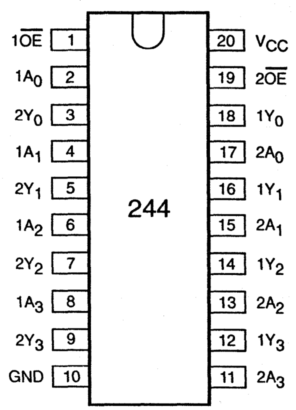


Fig.1 Pin configuration.

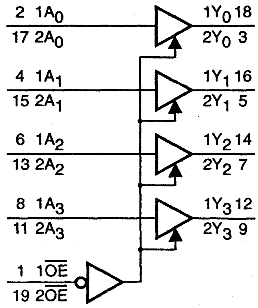


Fig.2 Logic symbol.

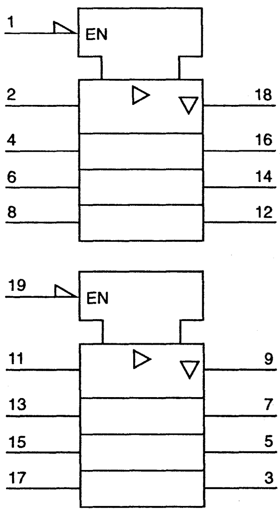


Fig.3 IEC logic symbol.

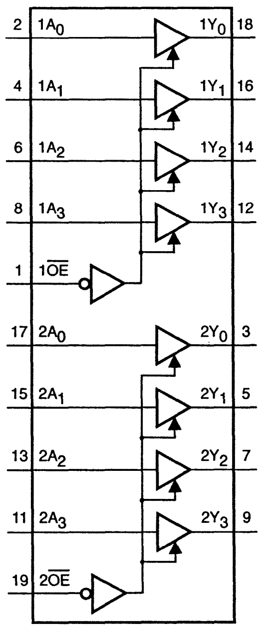


Fig.4 Functional diagram.

DC characteristics for 74LV244

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: bus driver
I_{CC} category: MSI

AC characteristics for 74LV244

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			-40 to +85		-40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	Propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	- - -	50 16 10	- 24 15	- - -	- 30 19	- - -	- 36 23	ns	1.2 2.0 3.0	Fig. 5
t_{PZH}/t_{PZL}	3-state output enable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$	- - -	65 21 13	- 32 20	- - -	- 40 25	- - -	- 48 30	ns	1.2 2.0 3.0	Fig. 6
t_{PHZ}/t_{PLZ}	3-state output disable time $1\overline{OE}$ to $1Y_n$; $2\overline{OE}$ to $2Y_n$	- - -	70 22 14	 30 20	- - -	- 35 24	- - -	- 41 28	ns	1.2 2.0 3.0	Fig. 6
t_{THL}/t_{TLH}	output transition time	- - -	25 8 5	- 16 10	- - -	- 20 13	- - -	- 24 15	ns	1.2 2.0 3.0	Fig. 5

AC WAVEFORMS

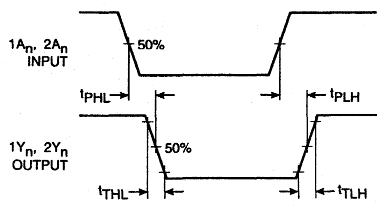


Fig. 5 Waveforms showing the input ($1A_n$, $2A_n$) to output ($1Y_n$, $2Y_n$) propagation delays and the output transition times.

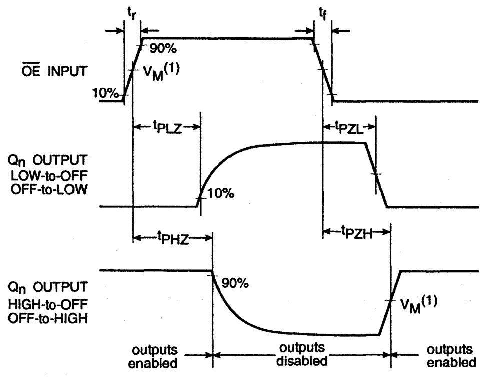


Fig.6 Waveforms showing the 3-state enable and disable times.

Note to the AC waveforms

(1) V_M = 50%; V_I = GND to V_{CC}.

FEATURES

- **Optimized for Low Voltage applications: 1.2 to 3.6 V**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV245 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HCT245.

The 74LV245 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The "245" features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUT	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 50 pF V_{CC} = 3.3 V	7	ns
C_I	input capacitance		3.0	pF
$C_{I/O}$	input/output capacitance		10	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV245N	20	DIL	plastic	DIL20/SOT146
74LV245D	20	SO	plastic	SO20/SOT163A
74LV245DB	20	SSOP	plastic	SSOP20/SOT339

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B_0 to B_7	data inputs/outputs
19	$\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive supply voltage

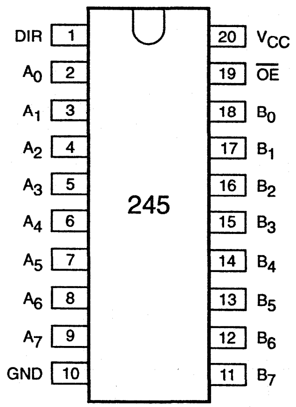


Fig.1 Pin configuration.

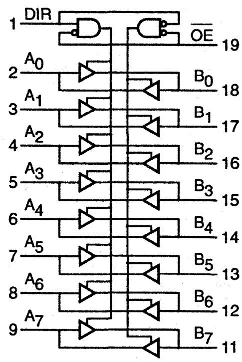


Fig.2 Logic symbol.

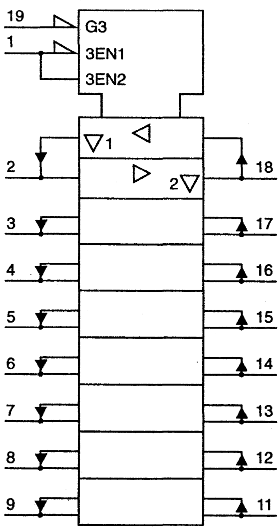


Fig.3 IEC logic symbol.

DC characteristics for 74LV245

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".

I_{CC} category: MSI

AC characteristics for 74LV245

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	− − −	45 15 9	− 23 14	− − −	− 28 18	− − −	− 34 21	ns	1.2 2.0 3.0	Fig.4
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$, DIR to A_n; $\overline{OE}$, DIR to B_n	− − −	55 18 11	− 28 17	− − −	− 35 21	− − −	− 43 26	ns	1.2 2.0 3.0	Fig.5
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$, DIR to A_n; $\overline{OE}$, DIR to B_n	− − −	55 22 15	− 30 20	− − −	− 37 24	− − −	− 43 28	ns	1.2 2.0 3.0	Fig.5
t_{THL}/t_{TLH}	output transition time	− − −	25 8 5	− 16 10	− − −	− 20 13	− − −	− 24 15	ns	1.2 2.0 3.0	Fig.4

AC WAVEFORMS

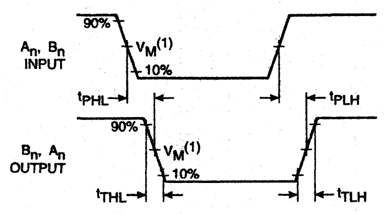


Fig. 4 Waveforms showing the input (A_n, B_n) to output (B_n, A_n) propagation delays and the output transition times.

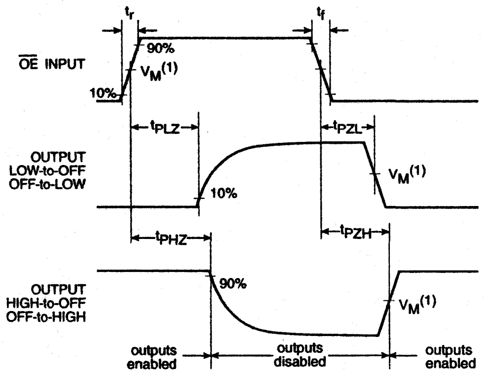


Fig.5 Waveforms showing the 3-state enable and disable times.

Note to the AC waveforms

(1) V_M = 50%; V_I = GND to V_{CC}.

Octal D-type flip-flop; positive-edge trigger 74LV273

FEATURES

- **Optimized for Low Voltage applications: 1.2 to 3.6 V**
- **Ideal buffer for MOS microprocessor or memory**
- **Common clock and master reset**
- **Eight positive edge-triggered D-type flip-flops**
- **Output capability: standard**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV273 a low-voltage Si-gate CMOS device and is pin and function compatible with 74HCT273.

The 74LV273 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{MR}$ input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n; $\overline{MR}$ to Q_n	C_L = 50 pF V_{CC} = 3.3 V	15 15	ns
f_{max}	maximum clock frequency		66	MHz
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV273N	20	DIL	plastic	DIL20/SOT146
74LV273D	20	SO	plastic	SO20/SOT163A

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	master reset input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

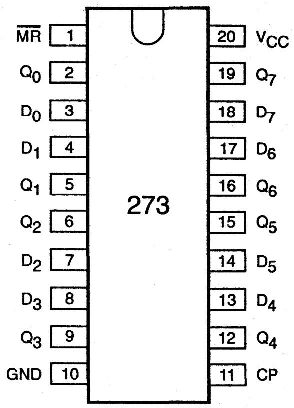


Fig.1 Pin configuration.

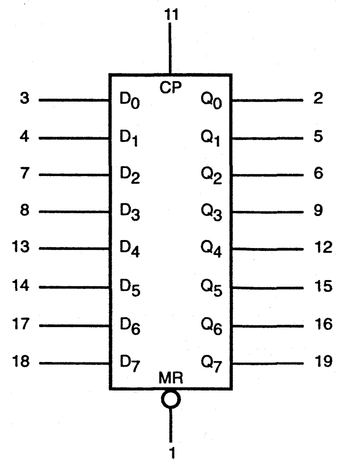


Fig.2 Logic symbol.

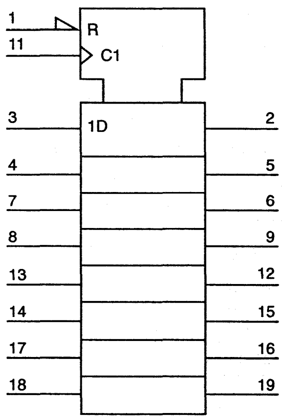


Fig3. IEC logic symbol.

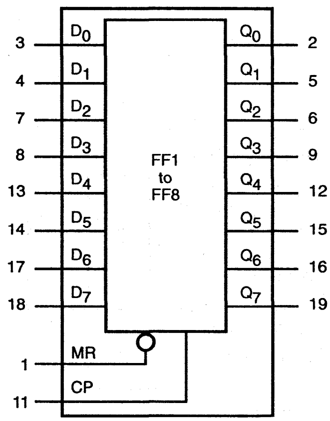


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_0 to Q_7
reset (clear)	L	X	X	L
load '1'	H	↑	h	H
load '0'	H	↑	l	L

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition
↑ = LOW-to-HIGH transition
X = don't care

DC characteristics for 74LV273

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
I_{CC} category: MSI

AC characteristics for 74LV273

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			-40 to +85		-40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	– – –	75 25 15	– 38 23	– – –	– 48 29	– – –	– 58 35	ns	1.2 2.0 3.0	Fig.5
t_{PHL}	propagation delay $\overline{MR}$ to Q_n	– – –	80 27 16	– 40 24	– – –	– 50 30	– – –	– 60 36	ns	1.2 2.0 3.0	Fig.6
t_{THL}/t_{TLH}	output transition time	– – –	25 8 5	– 16 10	– – –	– 20 13	– – –	– 24 15	ns	1.2 2.0 3.0	Fig.5
t_W	clock pulse width HIGH or LOW			– –		– –		– –	ns	2.0 3.0	Fig.5
t_W	master reset pulse width LOW			– –		– –		– –	ns	2.0 3.0	Fig.6
t_{rem}	removal time $\overline{MR}$ to CP	–		– – –	–	– – –	–	– – –	ns	1.2 2.0 3.0	Fig.6
t_{su}	set-up time D_n to CP	–		– – –	–	– – –	–	– – –	ns	1.2 2.0 3.0	Fig.7
t_h	hold time D_n to CP	–		– – –	–	– – –	–	– – –	ns	1.2 2.0 3.0	Fig.7
f_{max}	maximum clock pulse frequency			– –					ns	2.0 3.0	Fig. 5

AC WAVEFORMS

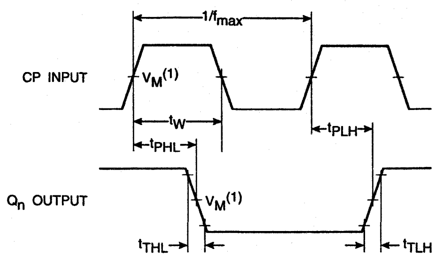


Fig.5 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

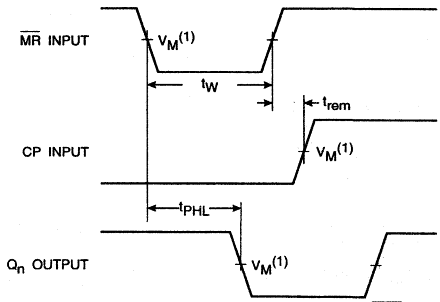


Fig.6 Waveforms showing master reset ($\overline{MR}$) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time.

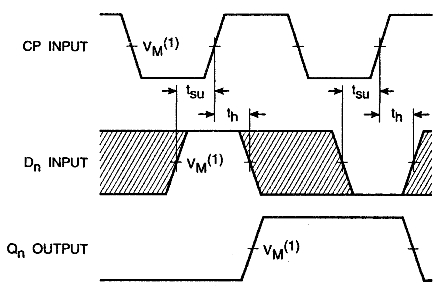


Fig.7 Waveforms showing the data set-up and hold times for the data input (D_n).

Note to Fig.7:

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to the AC waveforms

(1) V_M = 50%; V_I = GND to V_{CC}.

FEATURES

- **Optimized for Low Voltage applications: 1.2 to 3.6 V**
- **3-state non-inverting outputs for bus oriented applications**
- **Common 3-state output enable input**
- **Functionally identical to the '573'**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV373 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HCT373.

The 74LV373 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all internal latches.

The '373' consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The '373' is functionally identical to the '573', but the '573' has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n; LE to Q_n	C_L = 50 pF V_{CC} = 3.3 V	 12 15	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	45	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV373N	20	DIL	plastic	DIL20/SOT146
74LV373D	20	SO	plastic	SO20/SOT163A

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	3-state latch outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
20	V_{CC}	positive supply voltage

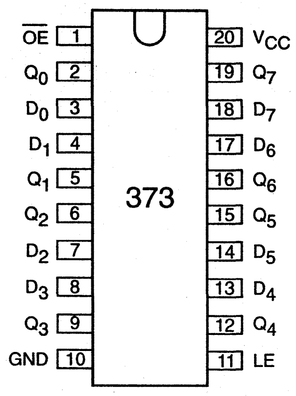


Fig.1 Pin configuration.

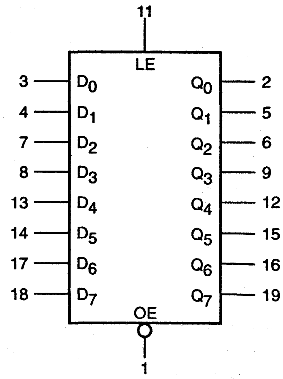


Fig.2 Logic symbol.

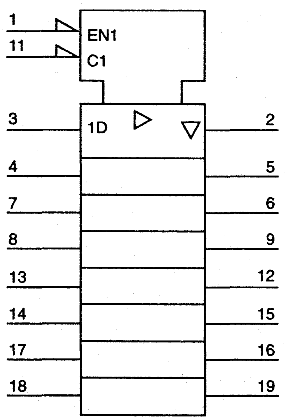


Fig3. IEC logic symbol.

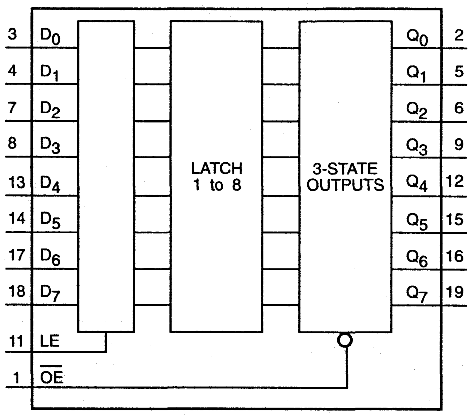


Fig.4 Functional diagram.

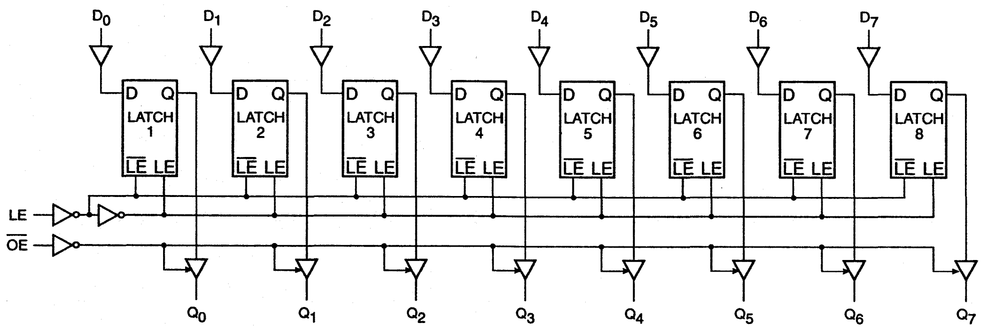


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_0 to Q_7
enable and read register (transparent mode)	L L	H H	L H	L H	L H
latch and read register	L L	L L	l h	L H	L H
latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
X = don't care
Z = high impedance OFF-state

DC characteristics for 74LV373

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
I_{CC} category: MSI

AC characteristics for 74LV373

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n	– – –	75 25 15	– 38 23	– – –	– 48 29	– – –	– 58 35	ns	1.2 2.0 3.0	Fig.6
t_{PHL}/t_{PLH}	propagation delay LE to Q_n	– – –	90 30 18	– 45 27	– – –	– 56 34	– – –	– 68 41	ns	1.2 2.0 3.0	Fig.7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	– – –	80 27 16	– 40 24	– – –	– 50 30	– – –	– 60 36	ns	1.2 2.0 3.0	Fig.9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	– – –	65 25 17	– 35 23	– – –	– 43 28	– – –	– 45 32	ns	1.2 2.0 3.0	Fig.9
t_{THL}/t_{TLH}	output transition time	– – –	25 8 5	– 16 10	– – –	– 20 13	– – –	– 24 15	ns	1.2 2.0 3.0	Fig. 6
t_W	LE pulse width HIGH			– –		– –		– –	ns	2.0 3.0	Fig.7
t_{su}	set-up time D_n to LE	–		– – –	–	– – –	–	– – –	ns	1.2 2.0 3.0	Fig.9
t_h	hold time D_n to LE	–		– – –	–	– – –	–	– – –	ns	1.2 2.0 3.0	Fig.9

AC WAVEFORMS

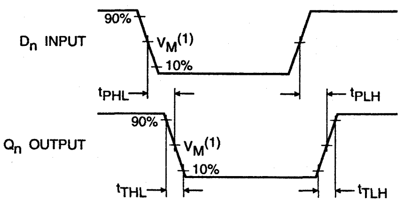


Fig.6 Waveforms showing the input (D_n) to output (Q_n) propagation delays and the output transition times.

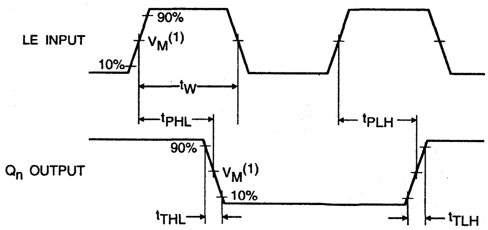


Fig.7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays and the output transition times.

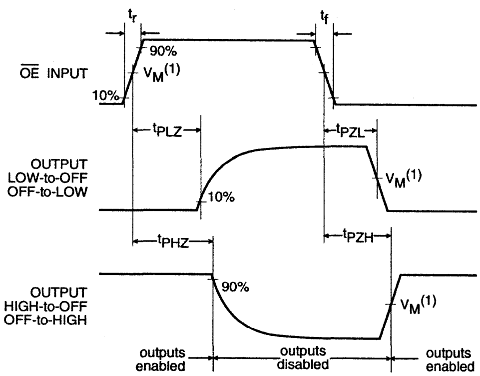


Fig.8 Waveforms showing the 3-state enable and disable times

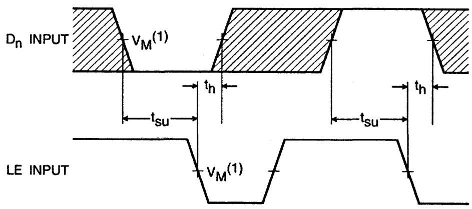


Fig.9 Waveforms showing the data set-up and hold times for the D_n input to the LE input.

Note to Fig.9:

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to the AC waveforms

(1) $V_M = 50\%$; V_I = GND to V_{CC}.

FEATURES

- **Optimized for Low Voltage applications: 1.2 to 3.6 V**
- **3-state non-inverting outputs for bus oriented applications**
- **8-bit positive edge-triggered register**
- **Common 3-state output enable input**
- **Independent register and 3-state buffer operation**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV374 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HCT374.

The 74LV374 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the eight flip-flops is available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 50 pF V_{CC} = 3.3 V	15	ns
f_{max}	maximum clock frequency		77	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	17	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV374N	20	DIL	plastic	DIL20/SOT146
74LV374D	20	SO	plastic	SO20/SOT163A
74LV374DB	20	SSOP	plastic	SSOP20/SOT339

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	3-state flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

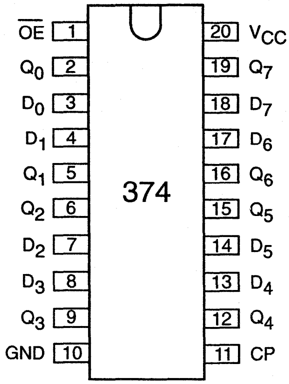


Fig.1 Pin configuration.

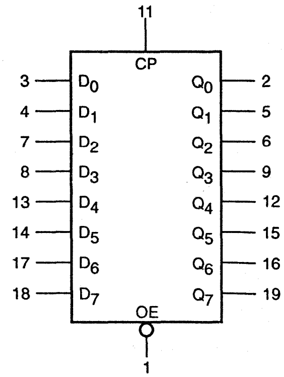


Fig.2 Logic symbol.

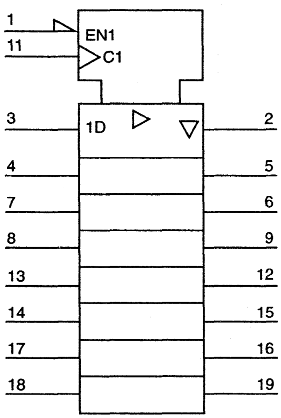


Fig3. IEC logic symbol.

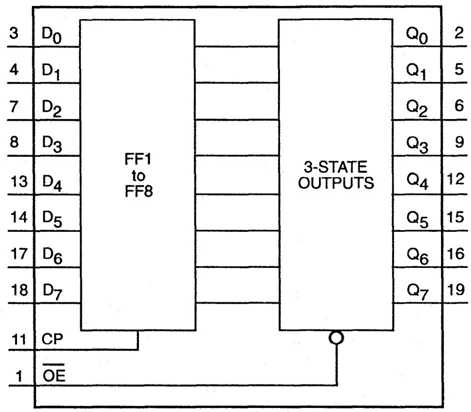


Fig.4 Functional diagram.

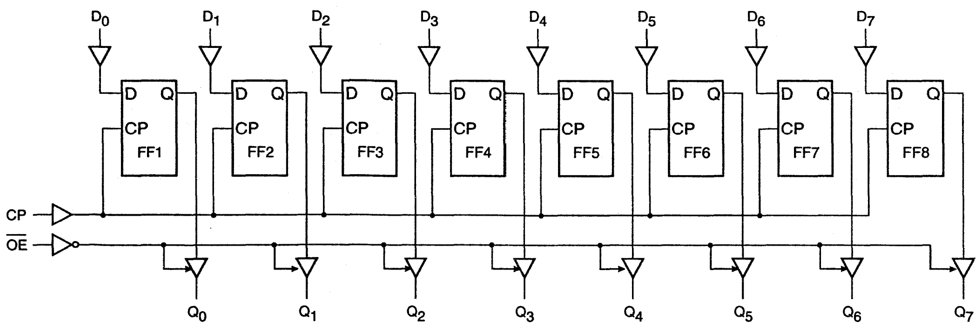


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0 to Q_7
load and read register	L L	↑ ↑	l h	L H	L H
load register and disable outputs	H H	↑ ↑	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition
Z = high impedance OFF-state

DC characteristics for 74LV374

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
I_{CC} category: MSI

AC characteristics for 74LV374

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	− − −	90 30 18	− 45 27	− − −	− 56 34	− − −	− 68 41	ns	1.2 2.0 3.0	Fig.6
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	− − −	75 25 15	− 38 23	− − −	− 48 29	− − −	− 58 35	ns	1.2 2.0 3.0	Fig.7
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	− − −	70 27 18	− 38 25	− − −	− 57 36	− − −	− 68 43	ns	1.2 2.0 3.0	Fig.7
t_{THL}/t_{TLH}	output transition time	− − −	25 8 5	− 16 10	− − −	− 20 13	− − −	− 24 15	ns	1.2 2.0 3.0	Fig. 6
t_W	clock pulse width HIGH or LOW	18 11	12 7	− −	23 14	− −	28 17	− −	ns	2.0 3.0	Fig.6
t_{su}	set-up time D_n to CP	− 13 8	25 8 5	− − −	− 17 10	− − −	− 20 12	− − −	ns	1.2 2.0 3.0	Fig.8
t_h	hold time D_n to CP	− −2 −2	−2 −2 −2	− − −	− −2 −2	− − −	− −2 −2	− − −	ns	1.2 2.0 3.0	Fig.8
f_{max}	maximum clock pulse frequency	27 46	42 70	− −	22 37	− −	18 31	− −	MHz	2.0 3.0	Fig.6

AC WAVEFORMS

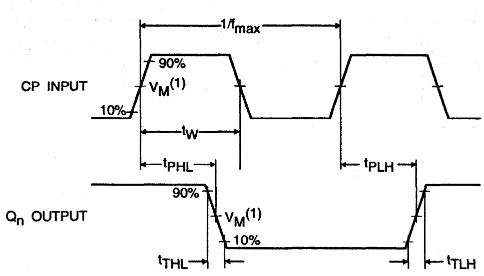


Fig.6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.

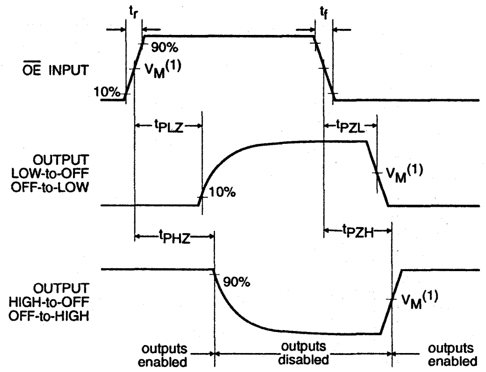


Fig.7 Waveforms showing the 3-state enable and disable times

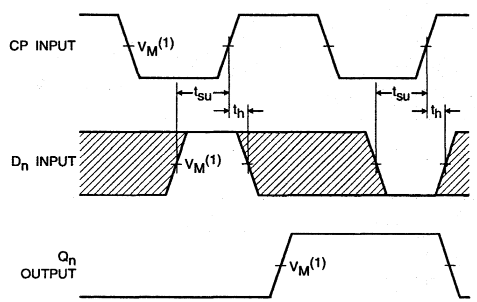


Fig.8 Waveforms showing the data set-up and hold times for the D_n input to the CP input.

Note to Fig.8:

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to the AC waveforms

(1) V_M = 50%; V_I = GND to V_{CC}.

Octal D-type transparent latch; 3-state — 74LV573

FEATURES

- **Optimized for Low Voltage applications: 1.2 to 3.6 V**
- **Inputs and outputs on opposite sides of package allowing easy interface with microprocessors**
- **Useful as input or output port for microprocessors/microcomputer**
- **3-state non-inverting outputs for bus oriented applications**
- **Common 3-state output enable input**
- **Functionally identical to the "563" and "373"**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

DESCRIPTION

The 74LV573 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) are common to all internal latches.

The "573" consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the eight latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The "573" is functionally identical to the "563" and the "373", but the "563" has inverted outputs and the "373" has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n; LE to Q_n	C_L = 15 pF V_{CC} = 3.3 V	14 15	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	26	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV573N	20	DIL	plastic	DIL20/SOT146
74LV573D	20	SO	plastic	SO20/SOT163A
74LV573DB	20	SSOP	plastic	SSOP20/SOT339

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
19, 18, 17, 16, 15, 14, 13, 12	Q_0 to Q_7	data outputs
20	V_{CC}	positive supply voltage

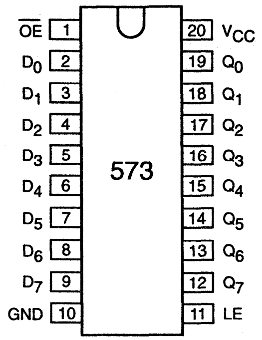


Fig.1 Pin configuration.

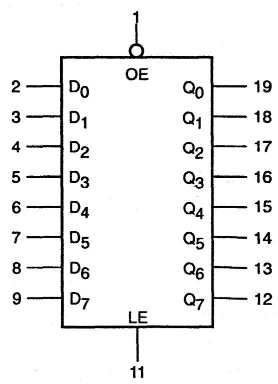


Fig.2 Logic symbol.

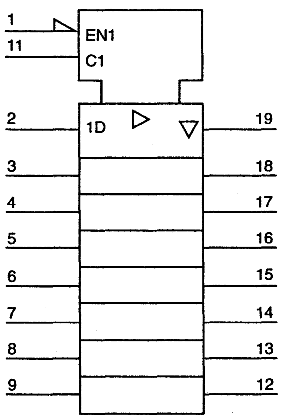


Fig.3 IEC logic symbol.

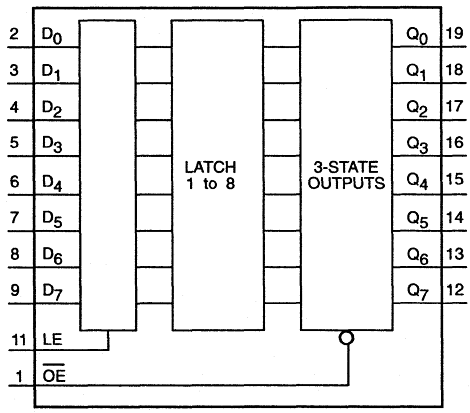


Fig.4 Functional diagram.

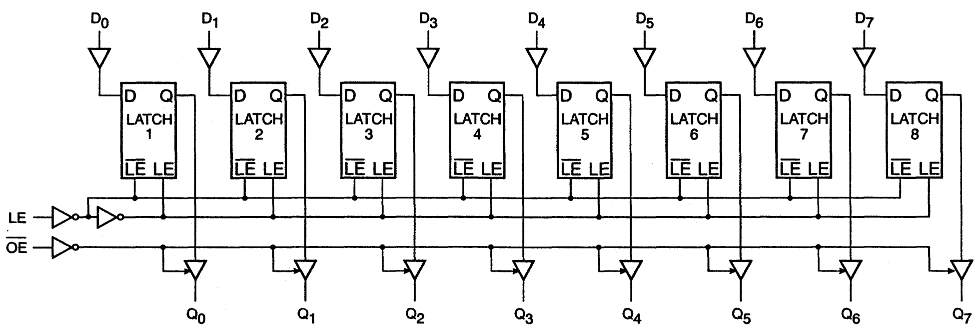


Fig.5 Logic diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_n		Q_0 to Q_7
enable and read register (transparent mode)	L L	H H	L H	L H	L H
latch and read register	L L	L L	l h	L H	L H
latch register and disable outputs	H H	L L	l h	L H	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
Z = high impedance OFF-state

DC characteristics for 74LV573

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
I_{CC} category: MSI

AC characteristics for 74LV573

GND = 0 V; $t_r = t_f = 2.0$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n	– – –	85 28 17	– 42 26	– – –	– 52 33	– – –	– 63 39	ns	1.2 2.0 3.0	Fig.6
t_{PHL}/t_{PLH}	propagation delay LE to Q_n	– – –	90 29 18	– 44 27	– – –	– 54 34	– – –	– 65 41	ns	1.2 2.0 3.0	Fig.7
t_{PZH}/t_{PZL}	3–state output enable time $\overline{OE}$ to Q_n	– – –	80 26 16	– 39 24	– – –	– 48 30	– – –	– 58 36	ns	1.2 2.0 3.0	Fig.8
t_{PHZ}/t_{PLZ}	3–state output disable time $\overline{OE}$ to Q_n	– – –	80 30 20	– 42 28	– – –	– 51 34	– – –	– 60 40	ns	1.2 2.0 3.0	Fig.8
t_{THL}/t_{TLH}	output transition time	– – –	35 10 7	– 20 15	– – –	– 25 19	– – –	– 30 23	ns	1.2 2.0 3.0	Fig.6
t_W	LE pulse width HIGH	– 25 16	25 8 5	– – –	– 32 20	– – –	– 38 24	– – –	ns	1.2 2.0 3.0	Fig.7
t_{su}	set–up time D_n to LE	– 16 10	20 7 4	– – –	– 20 13	– – –	– 24 15	– – –	ns	1.2 2.0 3.0	Fig.9
t_h	hold time D_n to LE	– 5 5	5 2 1	– – –	– 5 5	– – –	– 5 5	– – –	ns	1.2 2.0 3.0	Fig.9

AC WAVEFORMS

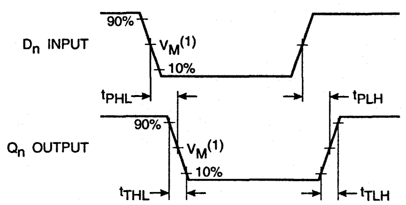


Fig.6 Waveforms showing the data input (D_n) to output (Q_n) propagation delays and the output transition times.

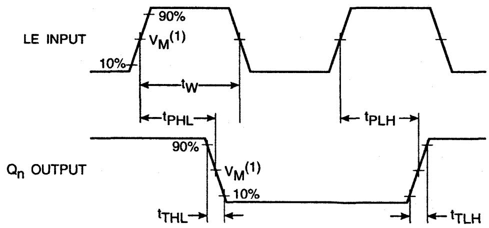


Fig.7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays and the output transition times.

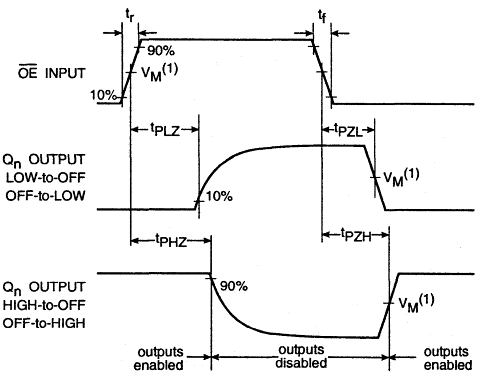


Fig.8 Waveforms showing the 3-state enable and disable times

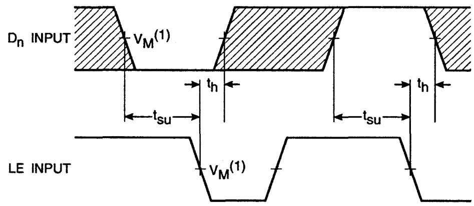


Fig.9 Waveforms showing the data set-up and hold times for the D_n input to the LE input.

Note to Fig.9:

The shaded areas indicate when the input is permitted to change for predictable output performance.

Note: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.

FEATURES

- **Optimized for Low Voltage applications: 1.2 to 6 V**
- **Very low "ON resistance:**
  25 Ω (typ.) at V_{CC} = 4.5 V
  35 Ω (typ.) at V_{CC} = 3.0 V
  65 Ω (typ.) at V_{CC} = 2.0 V
- **Output capability: standard**
- **I_{CC} category: SSI**

DESCRIPTION

The 74LV4066 is a low-voltage Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL).

The 74LV4066 has four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH enable input (nE). When nE is LOW the corresponding analog switch is turned off.

The 74LV4066 has an on resistance which is dramatically reduced in comparison with HC/HCT 4066.

FUNCTION TABLE

INPUTS	SWITCH
nE	
L	off
H	on

H = HIGH voltage level
L = LOW voltage level

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	turn-on time nE to V_{os}	C_L = 15 pF R_L = 1 kΩ V_{CC} = 3 V	11	ns
t_{PHZ}/t_{PLZ}	turn-on time nE to V_{os}		13	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	11	pF
C_S	maximum switch capacitances		8	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV4066N	14	DIL	plastic	DIL14/SOT27
74LV4066D	14	SO	plastic	SO14/SOT108A

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 8, 11	1Y to 4Y	independent inputs/outputs
2, 3, 9, 10	1Z to 4Z	independent inputs/outputs
13, 5, 6, 12	1E to 4E	enable input (active HIGH)
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

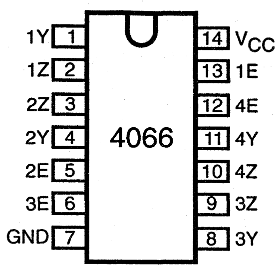


Fig.1 Pin configuration.

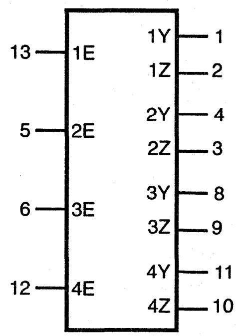


Fig.2 Logic symbol.

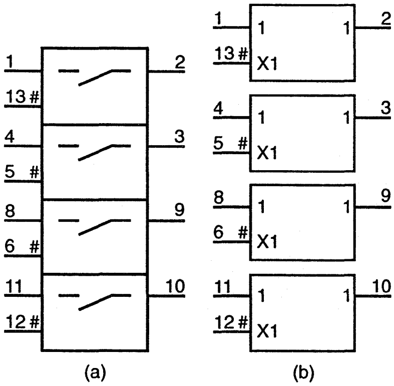


Fig.3 IEC Logic symbol.

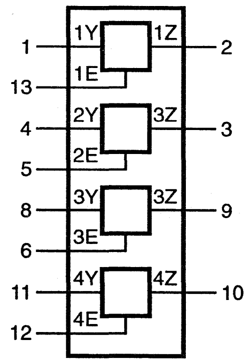


Fig.4 Functional diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7.0	V	
$\pm I_{IK}$	DC digital input diode current	–	20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{SK}$	DC switch diode current	–	20	mA	for $V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V
$\pm I_S$	DC switch current	–	25	mA	for -0.5 V $< V_S < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current	–	50	mA	
T_{stg}	storage temperature range	-65	+150	°C	
P_{tot}	power dissipation per package plastic DIL	–	750	mW	for temperature range: −40 to +125 °C above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)	–	500	mW	above +70 °C: derate linearly with 8 mW/K
P_S	power dissipation per switch	–	100	mW	

Note to the Ratings

To avoid drawing V_{CC} current out of terminal nZ, when switch current flows in terminal nY, the voltage drop accross the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no V_{CC} current will flow out of terminal nY. In this case there is no limit for the voltage drop accross the switch, but the voltages at nY and nZ may not exceed V_{CC} or GND

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	1.2	3.3	6.0	V	
V_I	DC input voltage range	GND	–	V_{CC}	V	
V_S	DC switch voltage range	GND	–	V_{CC}	V	
T_{amb}	operating ambient temperature range	−40	–	+85	°C	see DC and AC characteristics
T_{amb}	operating ambient temperature range	−40	–	+125	°C	see DC and AC characteristics
t_r, t_f	input rise and fall times	– – – –	– – – –	1000 700 500 250	ns	V_{CC} = 1.2 V V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V

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FEATURES

- **Optimized for Low Voltage applications: 1.2 to 3.6 V**
- **Output capability: standard**
- **I_{CC} category: MSI**

APPLICATIONS

- **Serial-to-parallel data conversion**
- **Remote control holding register**

DESCRIPTION

The 74LV4094 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HCT4094.

The 74LV4094 is an 8-stage serial shift registers having a storage latch associated with each stage for strobing data from the serial input (D) to the parallel buffered 3-state outputs (QP_0 to QP_7). The parallel outputs may be connected to the common bus lines. Data is shifted on the positive-going clock (CP) transitions. The data in each shift register is transferred to the storage register when the strobe input (STR) is HIGH. Data in the storage register appears at the outputs whenever the output enable input (OE) signal is HIGH.

Two serial outputs (QS_1 and QS_2) are available for cascading a number of '4094' devices. Data is available at QS_1 on the positive-going clock edges to allow high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information in available at QS_2 on the next negative going clock edge and is for cascading '4094' devices when the clock rise time is slow.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to QS_1 CP to QS_1 CP to QP_n STR to QP_n	C_L = 15 pF V_{CC} = 3.3 V	 15 13 20 18	ns
f_{MAX}	maximum clock frequency		95	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per gate	V_{CC} = 3.3 V notes 1 and 2	83	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV4094N	16	DIL	plastic	DIL16/SOT38Z
74LV4094D	16	SO	plastic	SO16/SOT109A

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	STR	strobe input
2	D	serial input
3	CP	clock input
4, 5, 6, 7, 14, 13, 12, 11	QP_0 to QP_7	parallel outputs
8	GND	ground (0 V)
9,10	QS_1, QS_2	serial outputs
15	OE	output enable input
16	V_{CC}	positive supply voltage

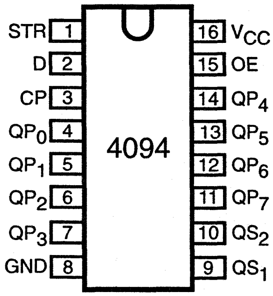


Fig.1 Pin configuration.

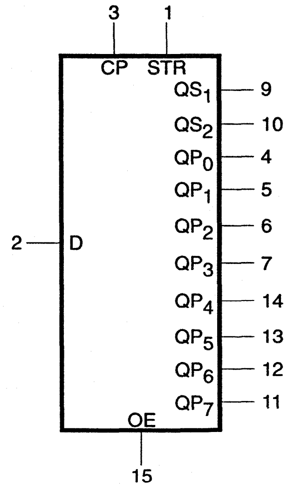


Fig.2 Logic symbol.

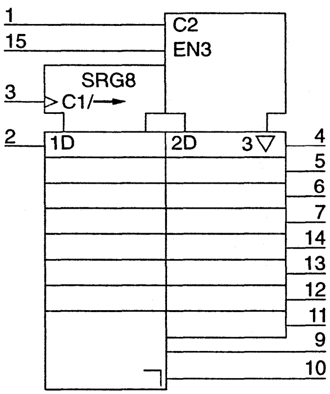


Fig.3 IEC logic symbol.

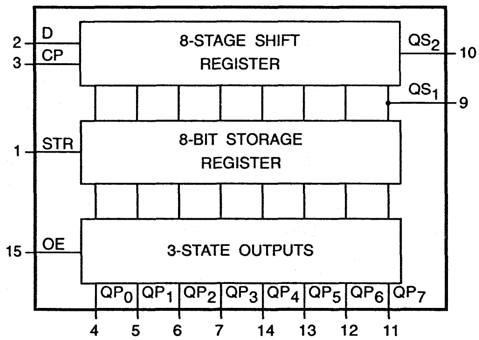


Fig.4 Functional diagram.

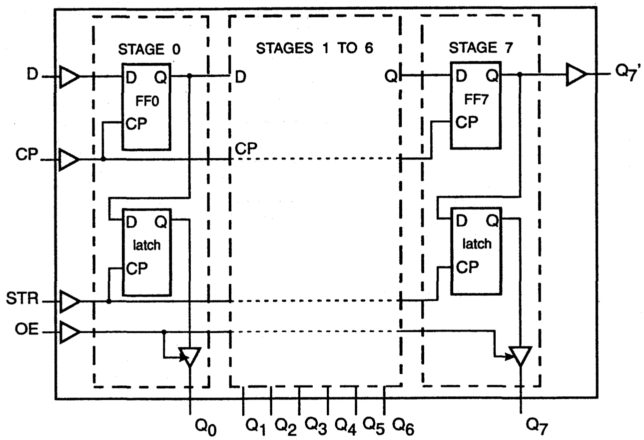


Fig.5 Logic diagram.

FUNCTION TABLE

INPUTS				PARALLEL OUTPUT		SERIAL OUTPUTS	
CP	OE	STR	D	QP_0	QP_n	QS_1	QS_2
↑	L	X	X	Z	Z	Q'_6	NC
↓	L	X	X	Z	Z	NC	QP_7
↑	H	L	X	NC	NC	Q'_6	NC
↑	H	H	L	L	QP_{n-1}	Q'_6	NC
↑	H	H	H	H	QP_{n-1}	Q'_6	NC
↓	H	H	H	NC	NC	NC	QP_7

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state
NC = no change

↑ = LOW-to-HIGH CP transition
↓ = HIGH-to-LOW CP transition
Q'_6 = the information in the seventh register stage is transferred to the 8th register stage and QS_n output at the positive clock edge.

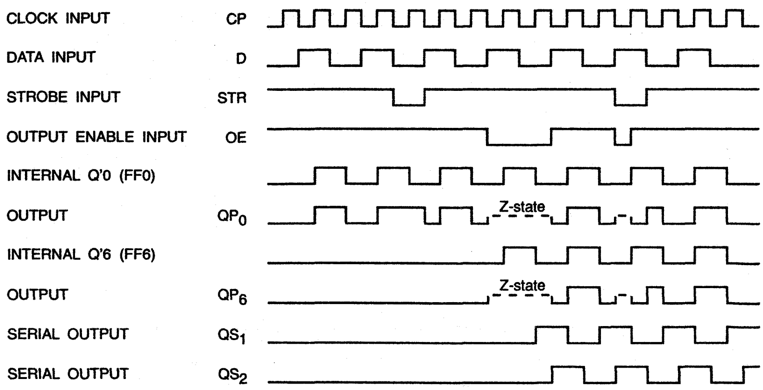


Fig.6 Timing diagram.

DC characteristics for 74LV4094

For the DC characteristics see chapter "LV family characteristics", section "Family specifications".
Output capability: standard
I_{CC} category: MSI

AC characteristics for 74LV4094

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.			
t_{PHL}/t_{PLH}	propagation delay CP to QS_1	− − −	90 30 18	− 45 27	− − −	− 57 34	− − −	− 68 41	ns	1.2 2.0 3.0	Fig.7
t_{PHL}/t_{PLH}	propagation delay CP to QS_2	− − −	80 27 16	− 40 24	− − −	− 50 30	− − −	− 60 36	ns	1.2 2.0 3.0	Fig.7
t_{PHL}/t_{PLH}	propagation delay CP to QP_n	− − −	115 38 23	− 58 35	− − −	− 73 44	− − −	− 88 53	ns	1.2 2.0 3.0	Fig.7
t_{PHL}/t_{PLH}	propagation delay STR to QP_n	− − −	105 35 21	− 53 32	− − −	− 67 40	− − −	− 80 48	ns	1.2 2.0 3.0	Fig.8
t_{PZH}/t_{PZL}	3-state output enable time OE to QP_n	− − −	100 33 20	− 50 30	− − −	− 63 38	− − −	− 75 45	ns	1.2 2.0 3.0	Fig.7
t_{PHZ}/t_{PLZ}	3-state output disable time OE to QP_n	− − −	55 21 15	− 30 20	− − −	− 37 24	− − −	− 43 28	ns	1.2 2.0 3.0	Fig.8
t_{THL}/t_{TLH}	output transition time	− − −	25 8 5	− 16 10	− − −	− 20 13	− − −	− 24 15	ns	1.2 2.0 3.0	Fig.5
t_W	clock pulse width HIGH or LOW	13 8	8 5	− −	17 10	− −	20 12	− −	ns	2.0 3.0	Fig.5
t_W	strobe pulse width; HIGH	13 8	8 5	− −	17 10	− −	20 12	− −	ns	2.0 3.0	Fig.6
t_{su}	set-up time D to CP	− 13 8	25 8 5	− − −	− 17 10	− − −	− 20 12	− − −	ns	1.2 2.0 3.0	Fig.10
t_{su}	set-up time CP to STR	− 25 15	50 17 10	− − −	− 32 19	− − −	− 38 23	− − −	ns	1.2 2.0 3.0	Fig.8
t_h	hold time D to CP	3 3 3	−10 −3 −2	− − −	3 3 3	− − −	3 3 3	− − −	ns	1.2 2.0 3.0	Fig.10
t_h	hold time CP to STR	0 0 0	−25 −8 −5	− − −	0 0 0	− − −	0 0 0	− − −	ns	1.2 2.0 3.0	Fig.8
f_{max}	maximum clock pulse frequency	35 58	52 87	− −	28 46	− −	23 39	− −	MHz	2.0 3.0	Fig.8

AC WAVEFORMS

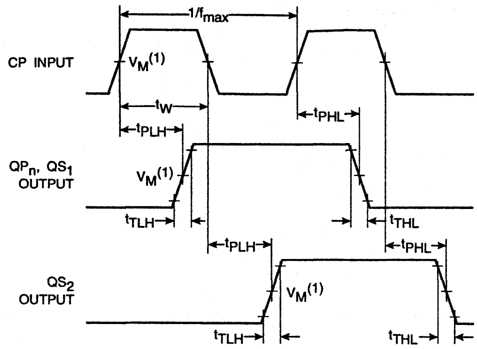


Fig.7 Waveforms showing the clock (CP) to output (QP_n, QS_1, QS_2) propagation delays, the clock pulse width and the maximum clock frequency.

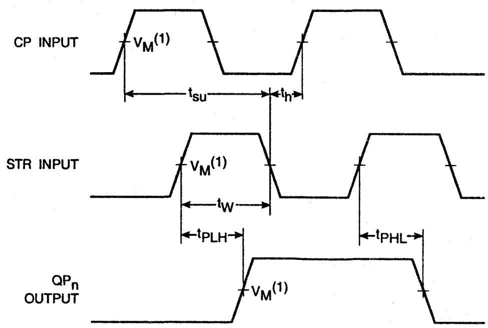


Fig.8 Waveforms showing the strobe (STR) to output (QP_n) propagation delays and the strobe pulse width and the clock set-up and hold times for the strobe input.

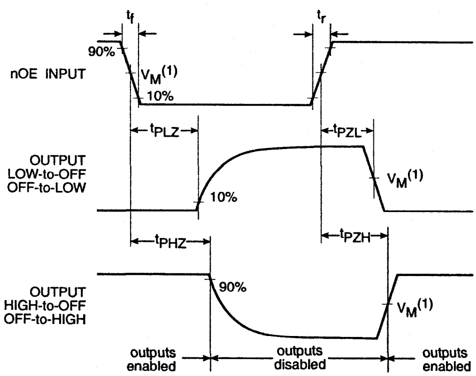


Fig.9 Waveforms showing the 3-state enable and disable times for input OE.

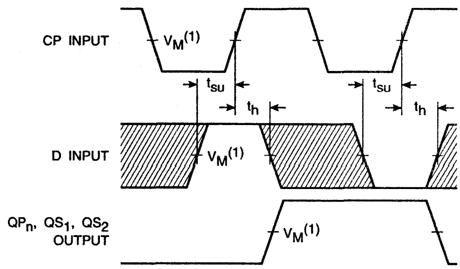


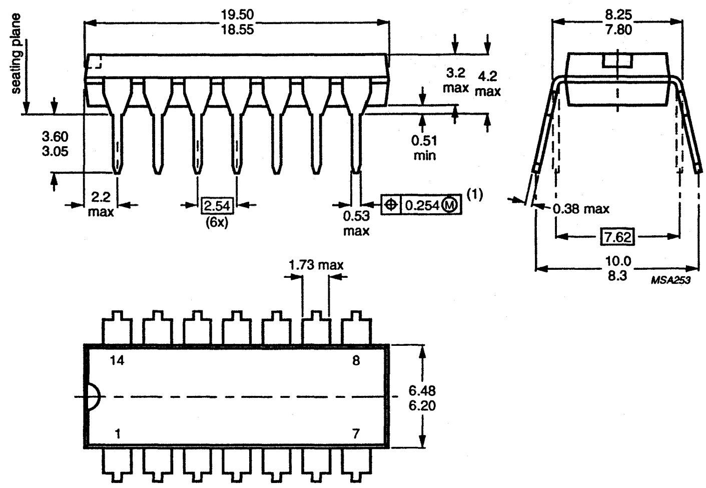
Fig.10 Waveforms showing the data set-up and hold times for the data input (D).

Note to Fig.10

The shaded areas indicate when the input is permitted to change for predictable output performance.

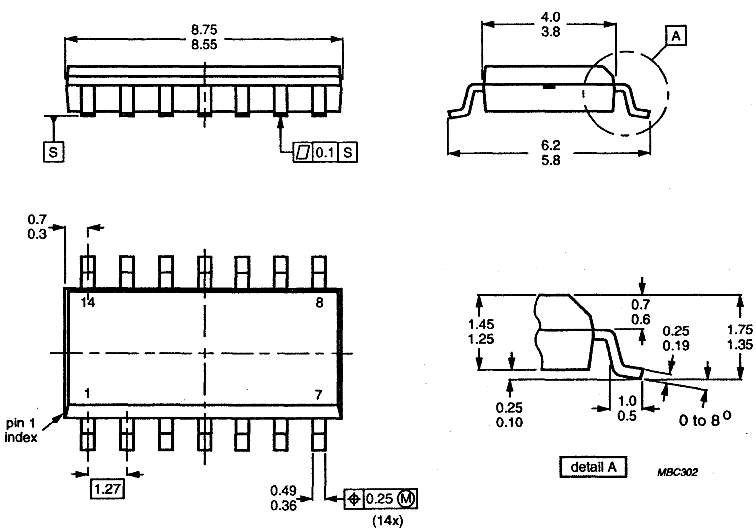
(1) V_M = 50%; V_I = GND to V_{CC}.

14-Lead dual in-line; plastic; SOT27

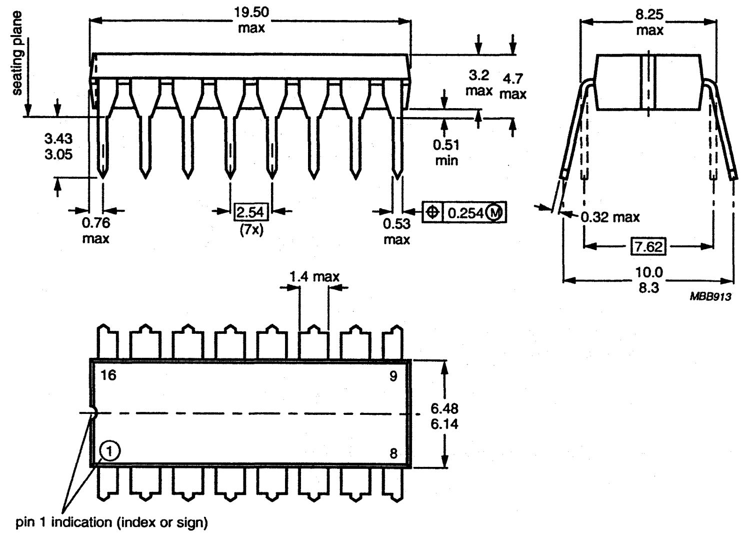


Dimensions in mm.

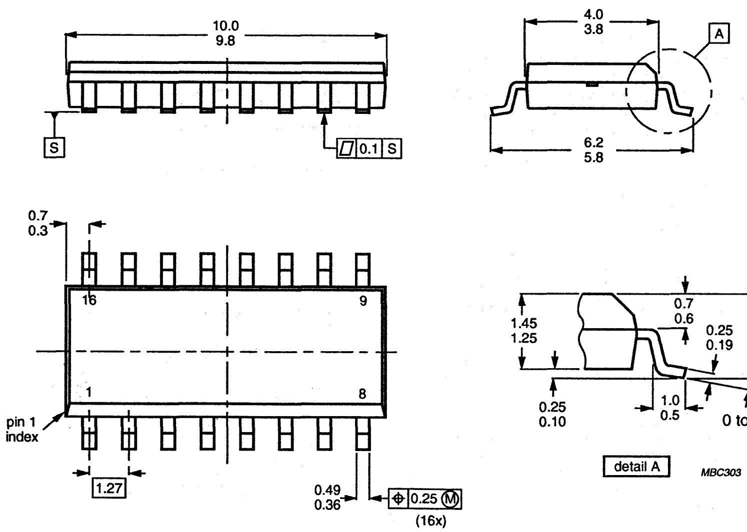
14-Lead mini-pack; plastic; SOT108A



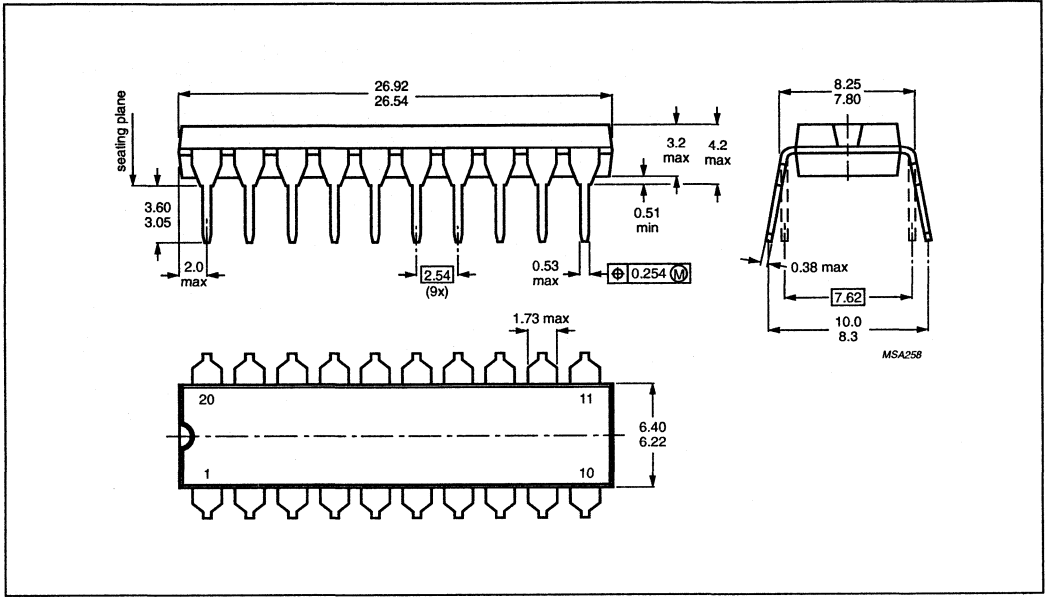
16-Lead dual in-line; plastic; SOT38Z



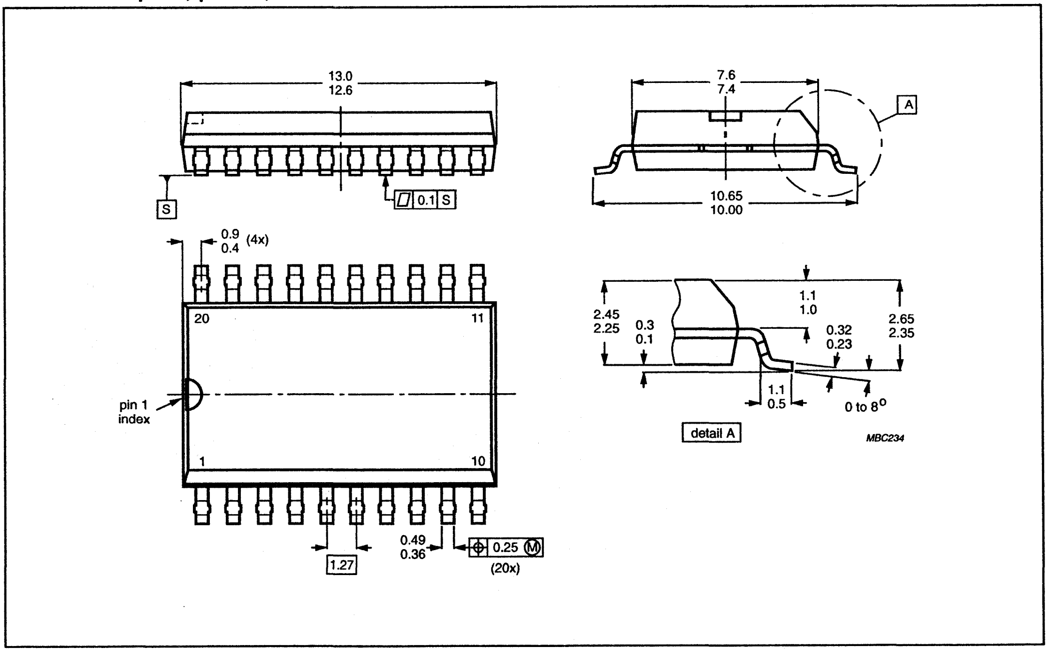
16-Lead mini-pack; plastic; SOT109A



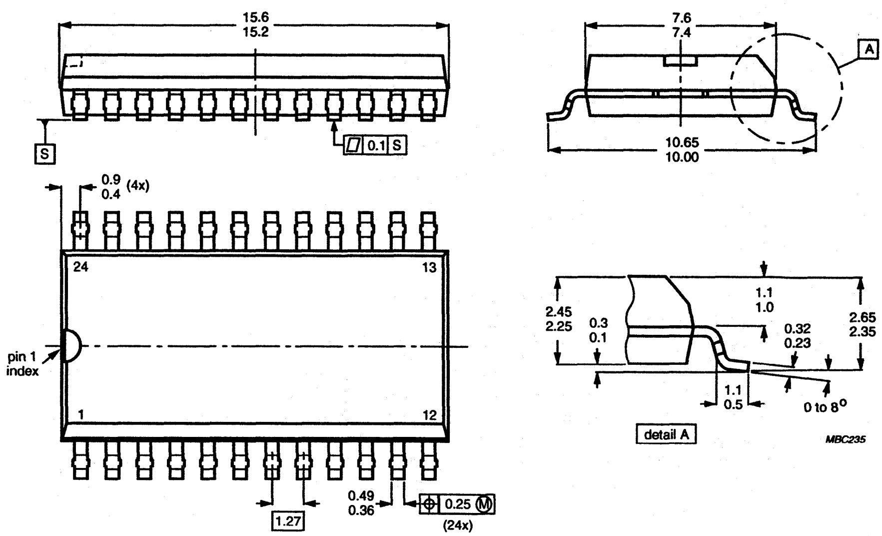
20-Lead dual in-line; plastic; SOT146



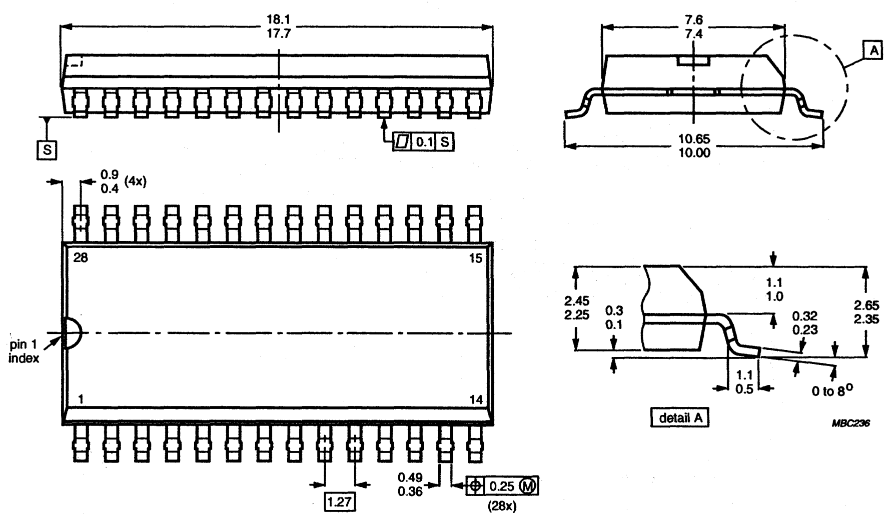
20-Lead mini-pack; plastic; SOT163A



24-Lead mini-pack; plastic; SOT137A



28-Lead mini-pack; plastic; SOT136A



SOLDERING

Plastic dual in-line

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

Plastic mini-packs

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

NOTES

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DATA HANDBOOK SYSTEM

Data handbook system

INTRODUCTION

Our data handbook system comprises more than 65 books with subjects including electronic components, subassemblies and magnetic products. The handbooks are classified into seven series:

- INTEGRATED CIRCUITS;
- DISCRETE SEMICONDUCTORS;
- DISPLAY COMPONENTS;
- PASSIVE COMPONENTS;
- PROFESSIONAL COMPONENTS;
- MAGNETIC PRODUCTS;
- LIQUID CRYSTAL DISPLAYS.

Data handbooks contain all pertinent data available at the time of publication and each is revised and reissued regularly.

Loose data sheets are sent to subscribers to keep them up-to-date on additions or alterations made during the lifetime of a data handbook.

Catalogues are available for selected product ranges (some catalogues are also on floppy discs).

For more information about data handbooks, catalogues and subscriptions, contact one of the organizations listed on the back cover of this handbook. Product specialists are at your service and enquiries are answered promptly.

INTEGRATED CIRCUITS

IC01	Semiconductors for Radio and Audio Systems
IC02	Semiconductors for Television and Video Systems
IC03	Semiconductors for Telecom Systems
IC04	CMOS HE4000B Logic Family
IC05	Advanced Low-power Schottky (ALS) Logic Series
IC06	High-speed CMOS Logic Family
IC08	ECL 100K ECL Logic Family
IC10	Memories
IC11	General Purpose/Linear ICs
IC12	Display Drivers and Microcontroller Peripherals

INTEGRATED CIRCUITS (continued)

IC13	Programmable Logic Devices (PLD)
IC14	8048-based 8-bit Microcontrollers
IC15	FAST TTL Logic Series
IC16	ICs for Clocks and Watches
IC18	Semiconductors for In-Car Electronics and General Industrial Applications
IC19	Semiconductors for Datacom: LANs, UARTs, Multi-Protocol Controllers and Fibre Optics
IC20	8051-based 8-bit Microcontrollers
IC21	68000-based 16-bit Microcontrollers
IC22	ICs for Multi-Media Systems
IC23	QUBIC Advanced BiCMOS Interface Logic ABT, MULTIBYTE™
IC24	Low Voltage CMOS Logic

DISCRETE SEMICONDUCTORS

SC01	Diodes
SC02	Power Diodes
SC03	Thyristors and Triacs
SC04	Small Signal Transistors
SC05	Low-frequency Power Transistors and Hybrid IC Power Modules
SC06	High-voltage and Switching Power Transistors
SC07	Small-signal Field-effect Transistors
SC08a	RF Power Bipolar Transistors
SC08b	RF Power MOS Transistors
SC09	RF Power Modules
SC10	Surface Mounted Semiconductors
SC12	Optocouplers
SC13	PowerMOS Transistors
SC14	Wideband Transistors and Wideband Hybrid IC Modules
SC15	Microwave Transistors
SC16	Wideband Hybrid IC Modules
SC17	Semiconductor Sensors

Data handbook system

DISPLAY COMPONENTS

- DC01 Colour Display Components
  Colour TV Picture Tubes and Assemblies
  Colour Monitor Tube Assemblies
- DC02 Monochrome Monitor Tubes and Deflection Units
- DC03 Television Tuners, Coaxial Aerial Input Assemblies
- DC04 Loudspeakers
- DC05 Flyback Transformers, Mains Transformers and General-purpose FXC Assemblies

PASSIVE COMPONENTS

- PA01 Electrolytic Capacitors
- PA02 Varistors, Thermistors and Sensors
- PA03 Potentiometers and Switches
- PA04 Variable Capacitors
- PA05 Film Capacitors
- PA06 Ceramic Capacitors
- PA07 Quartz Crystals for Special and Industrial Applications
- PA08 Fixed Resistors
- PA10 Quartz Crystals for Automotive and Standard Applications
- PA11 Quartz Oscillators

PROFESSIONAL COMPONENTS

- PC01 High-power Klystrons and Accessories
- PC02 Cathode-ray Tubes
- PC03 Geiger-Müller Tubes
- PC04 Photo Multipliers
- PC05 Plumbicon Camera Tubes and Accessories
- PC06 Circulators and Isolators
- PC07 Vidicon and Newvicon Camera Tubes and Deflection Units
- PC08 Image Intensifiers
- PC09 Dry-reed Switches
- PC11 Solid-state Image Sensors and Peripheral Integrated Circuits
- PC12 Electron Multipliers

MAGNETIC PRODUCTS

- MA01 Soft Ferrites
- MA02 Permanent Magnets
- MA03 Piezoelectric Ceramics
  Specialty Ferrites

LIQUID CRYSTAL DISPLAYS

- LCD01 Liquid Crystal Displays and Driver ICs for LCDs

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